AUTOMATIC PLACE AND ROUTE IN SILICON ENSEMBLE USING DEF

Type the following command to invoke the tool.
hostname.ece.pdx.edu> sedsm –m &
The "Silicon Ensemble" window should appear as shown in Fig1.

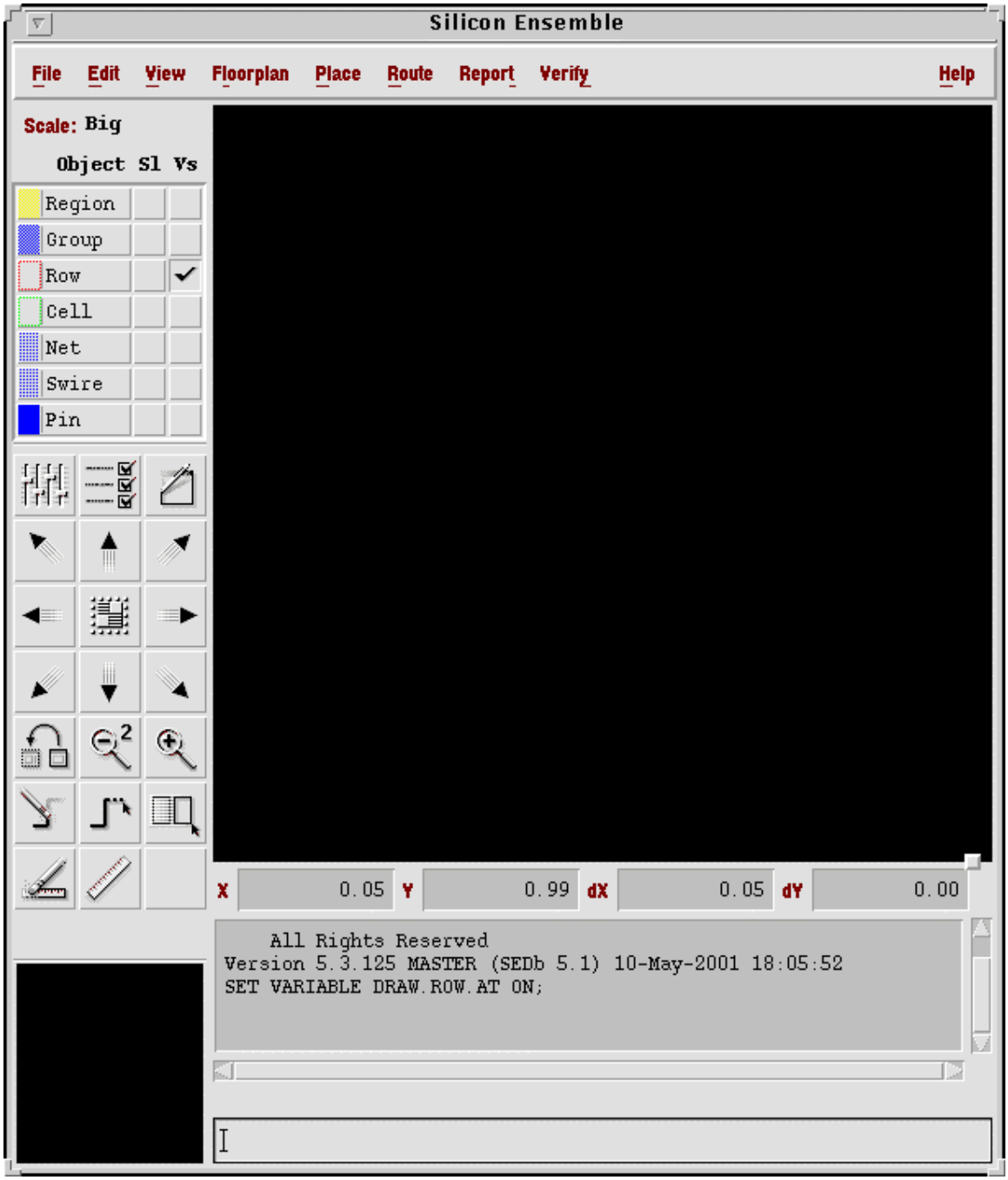

Fig 1: Silicon Ensemble Window

Importing LEF and DEF Files:

Click on ***File -> Import -> LEF*** in the "Silicon Ensemble" window .This brings up the "Import LEF" form as shown in Fig 2.
Select the .lef file and import it as shown in Fig 2.

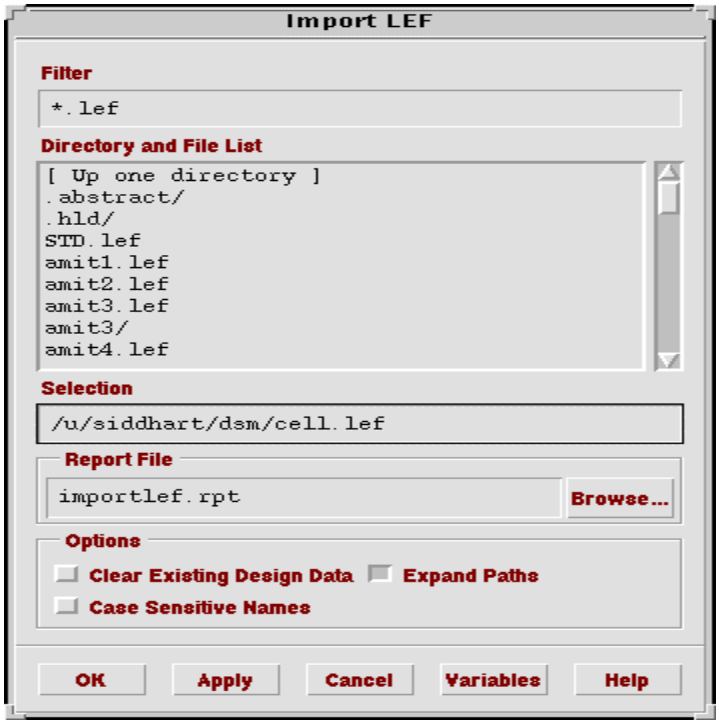

Fig 2: Import LEF

Click on ***File -> Import -> DEF*** in the art work window. This brings up "Import DEF" form as shown in Fig 3.Choose design directory as your path as shown in Fig 3.

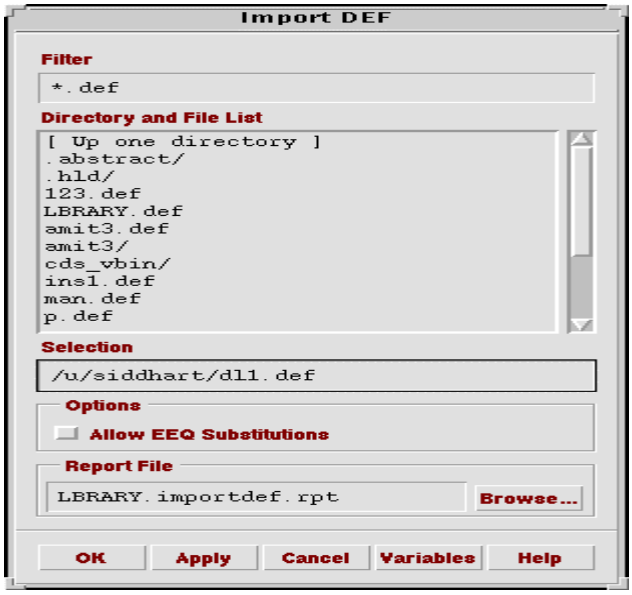

Fig 3: Import DEF

Initialize Floorplan:

Click on ***Floorplan-> Initialize Floorplan*** .This brings up "Initialize Floorplan" form. Fill the form as shown in Fig 4.

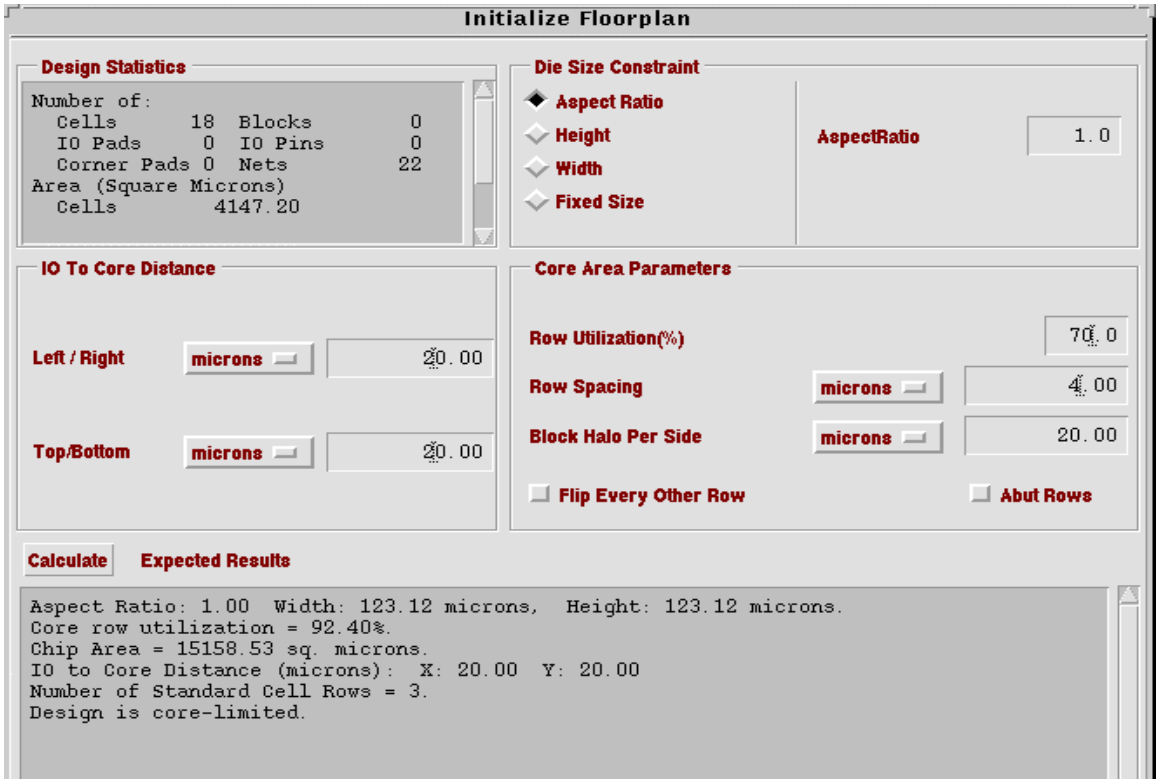

Fig 4: Initialize Floorplan

Fill the **IO To Core Distance** as 20 microns both for **Top/ Bottom** and **Left / Right**.
Fill the **Row Spacing** to 4 to 5 microns.
For **Row Utilization (%)** starting from 80% and run placement (PLACE Cells) .If the cells are placed then its fine otherwise repeat the step by decreasing the value of row utilization. .The floorplan will appear in the Silicon Ensemble window as shown in Fig 5

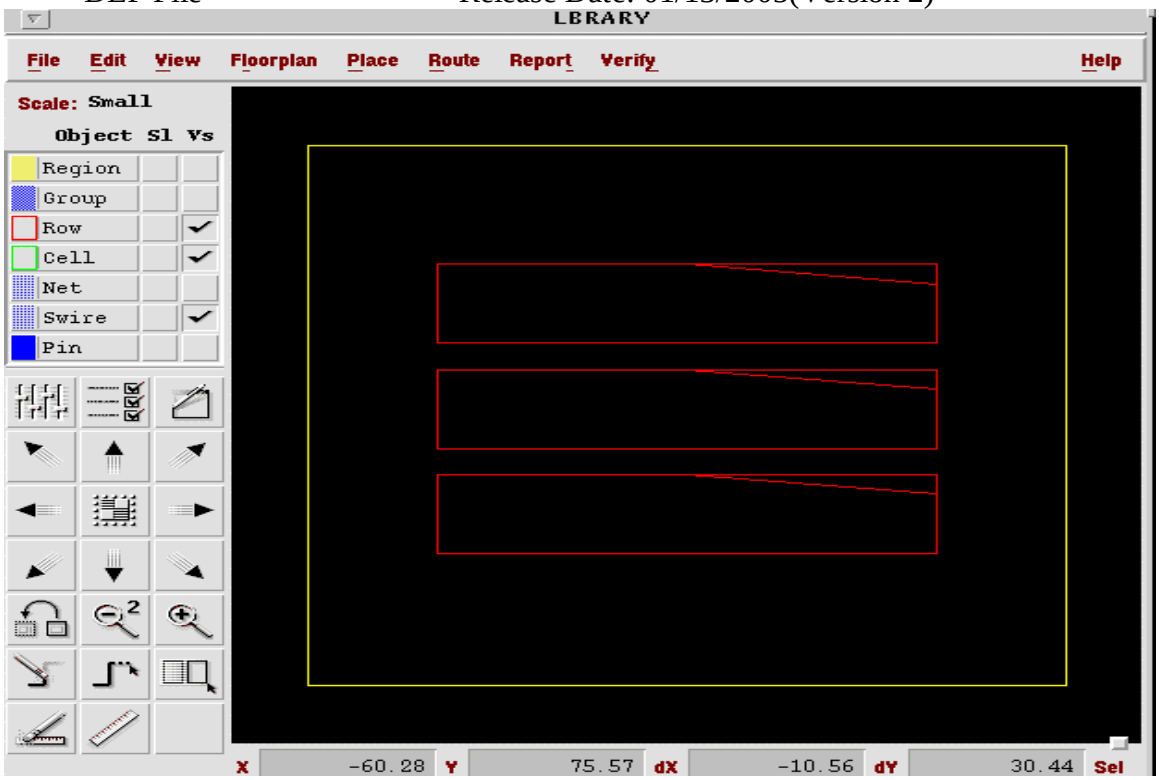

Fig 5: Rows after Floorplanning

ADD IO PINS:

The pins are added as the schematic of the design contains the logical pins.
In the Art work window click on EDIT -> Add -> Pin. This brings up “Add Pin” form. In the form fill as follows.
Select **NET TYPE** as **Special** for all vdd! and gnd! Pins.
Select **NET TYPE** as **Regular** for all other pins.
Select Use as **Power** for vdd! and Dir **INPUT**.
Select Use as **Ground** for gnd! And Dir **INPUT**.
Select Use as **Signal** for all input pins and Dir **INPUT**
Select Use as **Signal** for all output pins and Dir **OUTPUT**.
Write the name of pin (e.g. *vdd!*) in the Net Name and others entries as mentioned above.
Click on pick and then point and then click within the boundary of the Silicon Ensemble window .Then click ***OK*** .Complete this for all the pins.

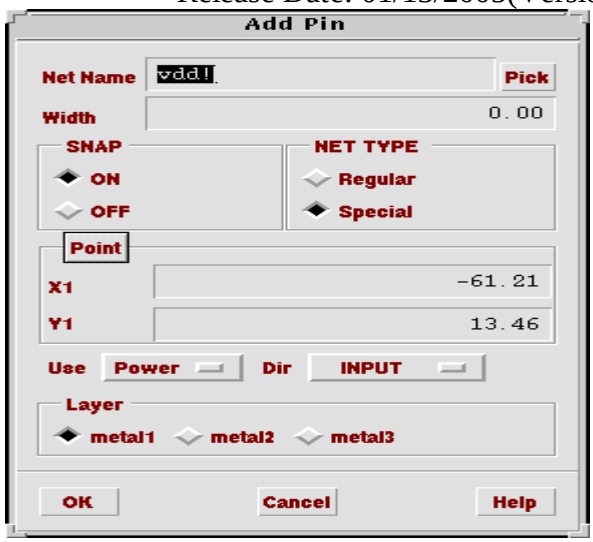

Fig 6: Add Pin

Edit property Global Signal pins vdd! and gnd!:

Edit the properties of the special nets as they are routed through abutment so change their shape to abutment .To chance the properties click on the pin object on the window and then click on the vdd! and gnd! pins on the routed view. Then hit ctrl + q together .The "Edit Properties" form appears as follows. Change the shape from NORMAL to ABUTMENT as shown in Fig 7.

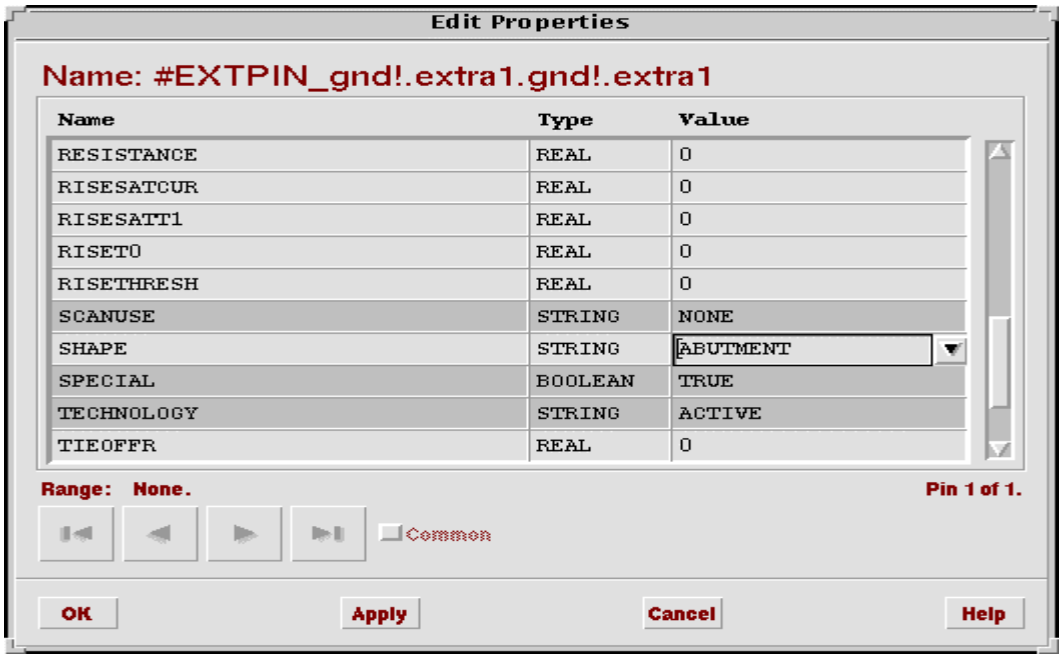

Fig 7: Edit Properties

Place IO:

In the Silicon Ensemble window click ***Place -> IO***. Choose Random and Evenly space as shown in Fig 8.

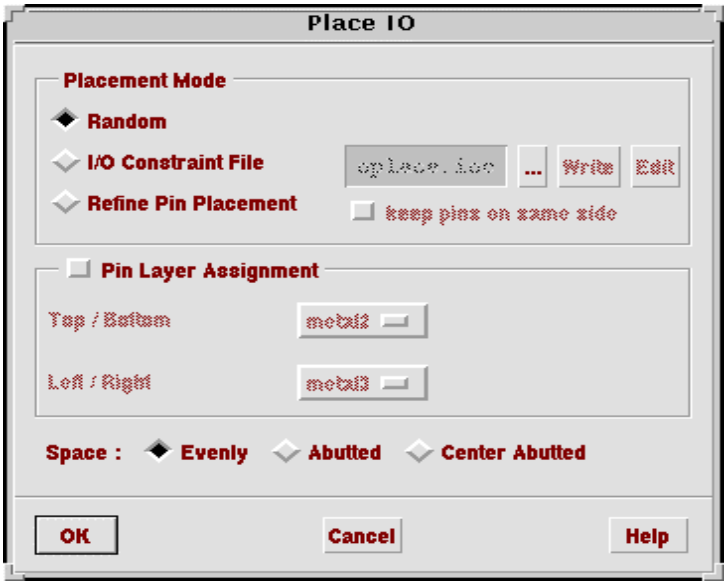

Fig 8: Place IO

Place Cells:

Choose Place Cells in the SE window. This brings up “Place Cells” form . In the form click ***OK***.

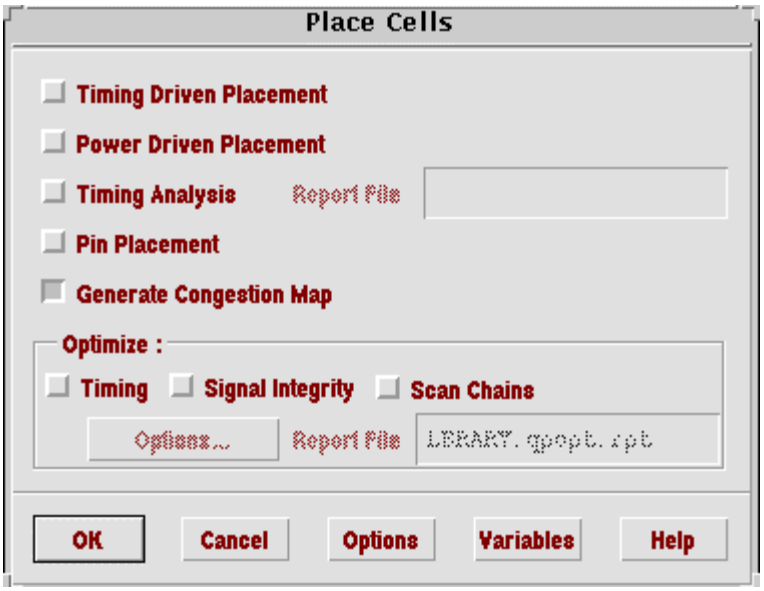

Fig 9: Place Cells

This will place the cells as shown in Fig 10.

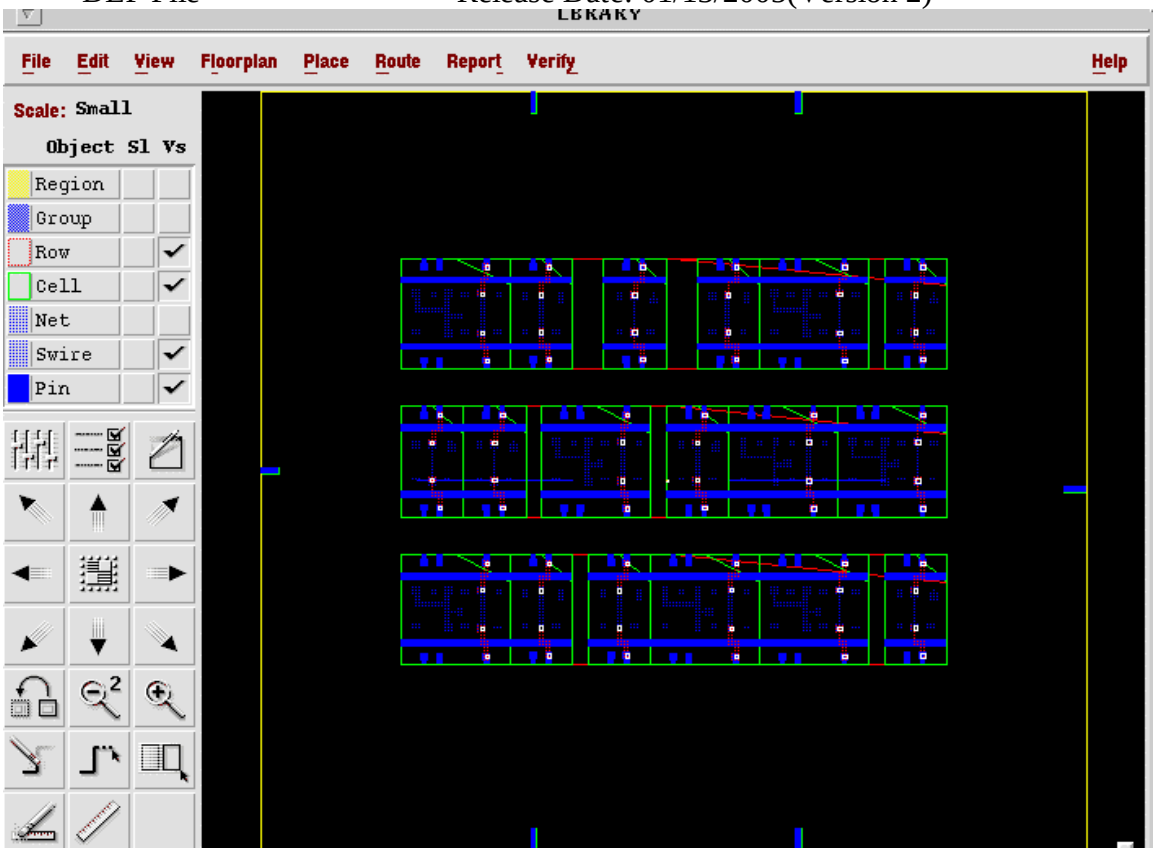

Fig 10: IO Pins and Cells Placed

Power Routing:

Click on ***Route ->Plan Power***
Click on **Add Rings** as shown in Fig 11.

Fig 11: Plan Power (PP)

This brings up “PP Add Rings” form as shown in Fig 12.
Fill **Core Ring Width** for both Metal1 and Metal2 as shown in Fig 12.Click **OK**

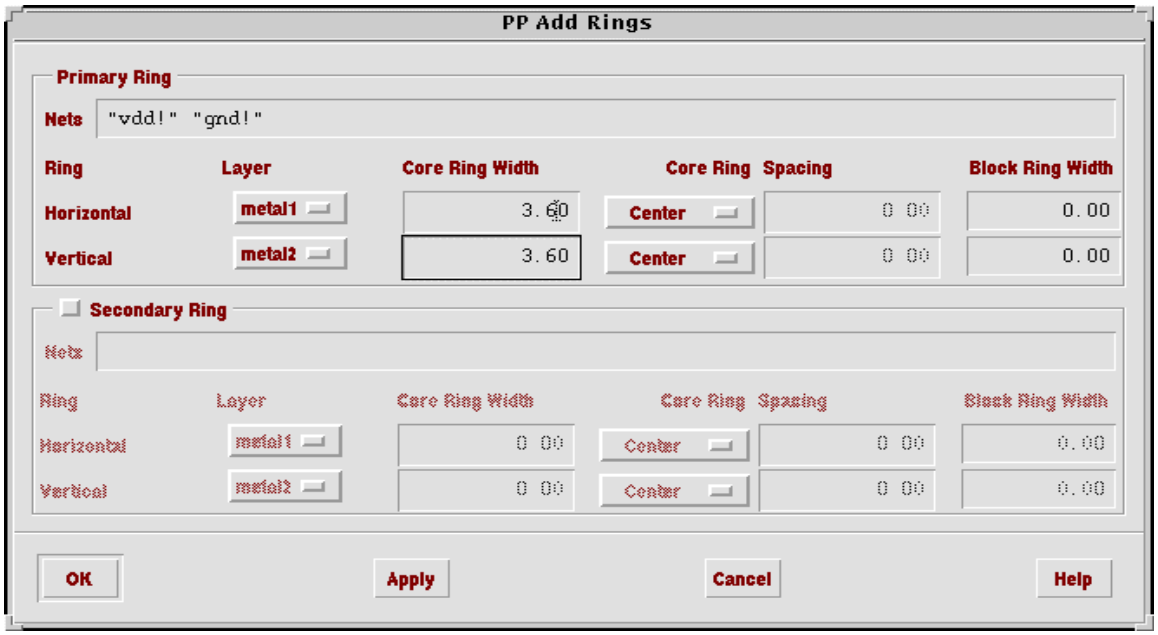

Fig 12: PP Add Rings

The Silicon Ensemble window appears as follows (Fig 13).

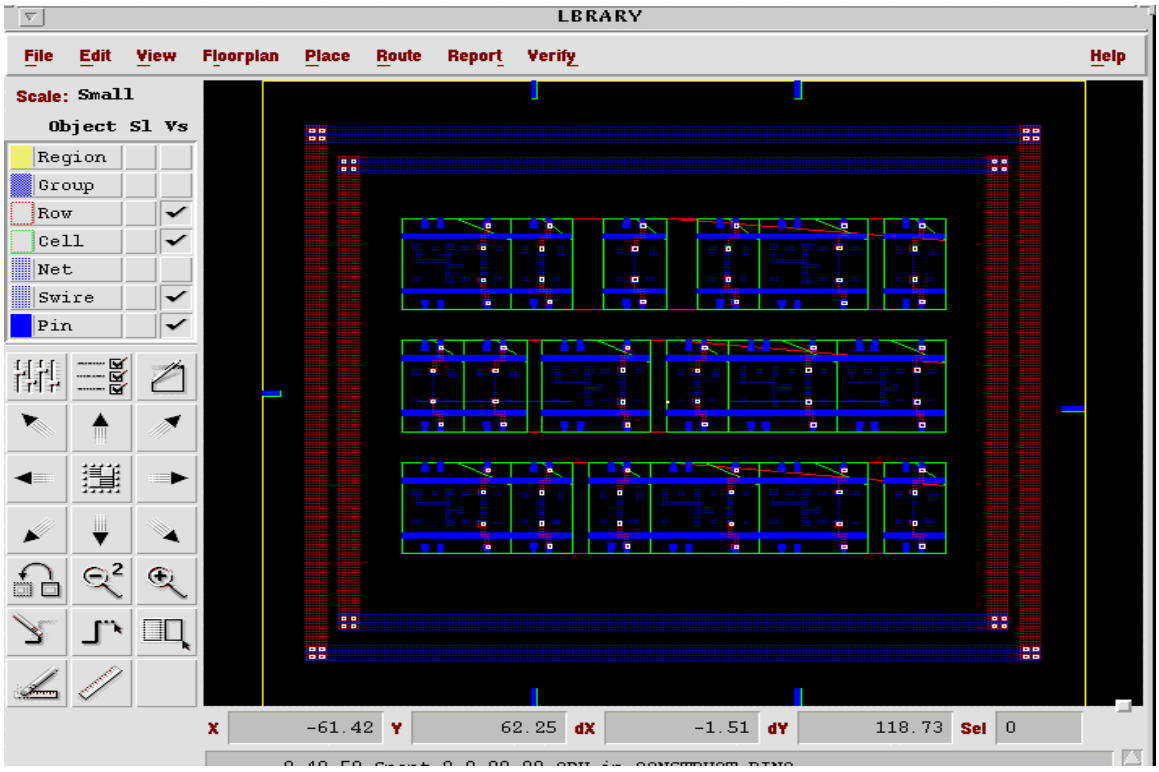

Fig 13: Cells with Power and Ground Rings

Then Click on ***Route-> Connect Ring*** .This brings up the “Connect Ring” form. Make sure you have vdd! and gnd! in the Nets as shown in Fig 14. Leave all settings as default .Click ***OK.***

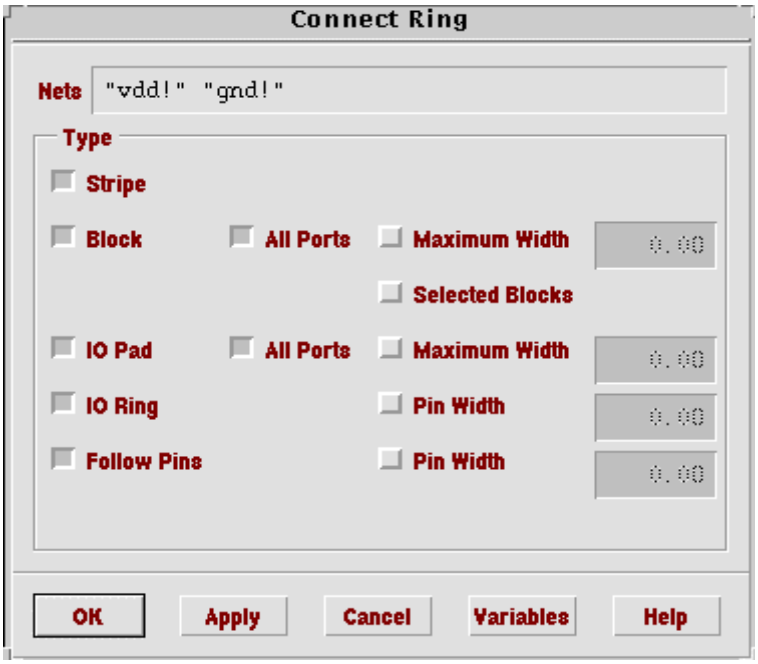

Fig 14: Connect Ring

The Silicon Ensemble window appears as shown in Fig 15.

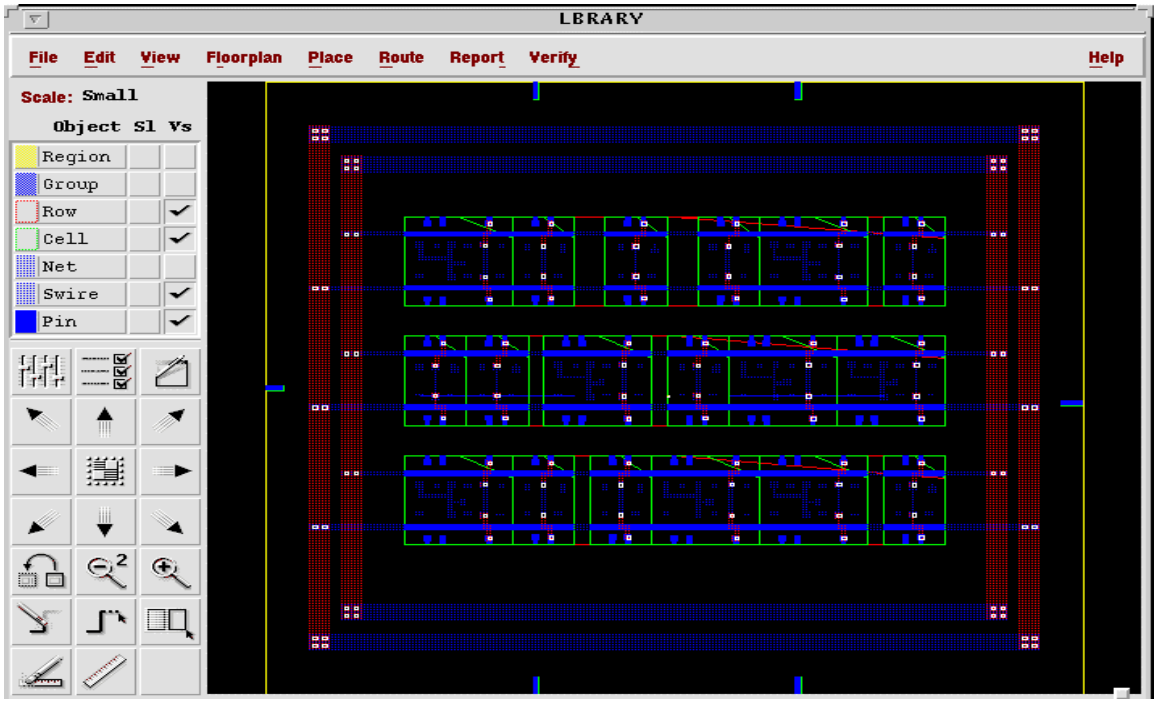

Fig 15: Cells with connected Rings

Signal Routing:

In the Silicon Ensemble window click ***Route -> Wroute.*** This brings up the
Make sure that both **Global and Final Route** and **Auto Search And Repair** are enabled.
Click ***OK***.

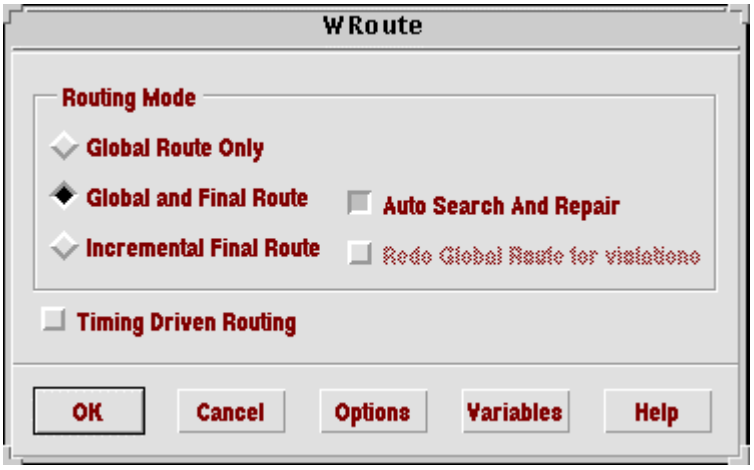

Fig 16: WRoute

Silicon Ensemble window appears as shown in Fig 17.

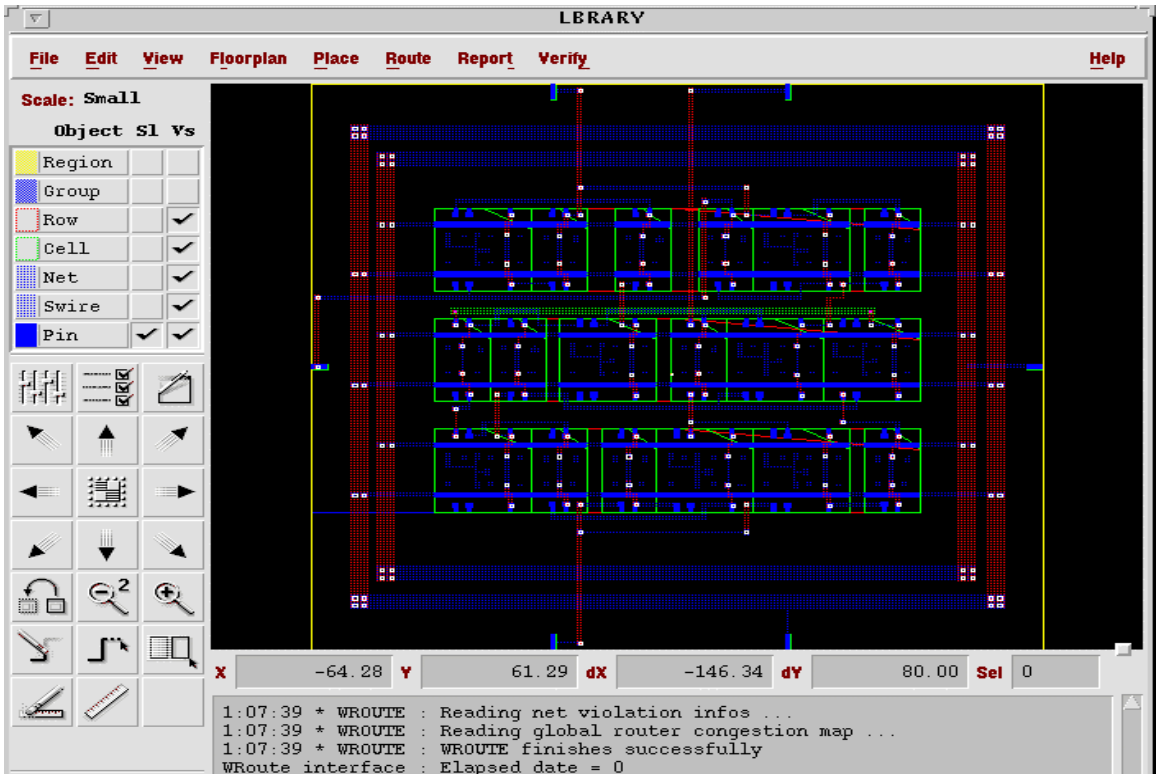

Fig 17: Cells after signal routing

Exporting the Design:

In the Silicon Ensemble window click ***File -> Export -> GDSII.***
Enable **GDS-II File** and fill the section with a file name with extension .gds2 (e.g. *LBRARY.gds2*).
Enable **Map File** and give it path
/home/ece/username/dsm/gds2.map
as shown in Fig 18.
Click ***OK***.

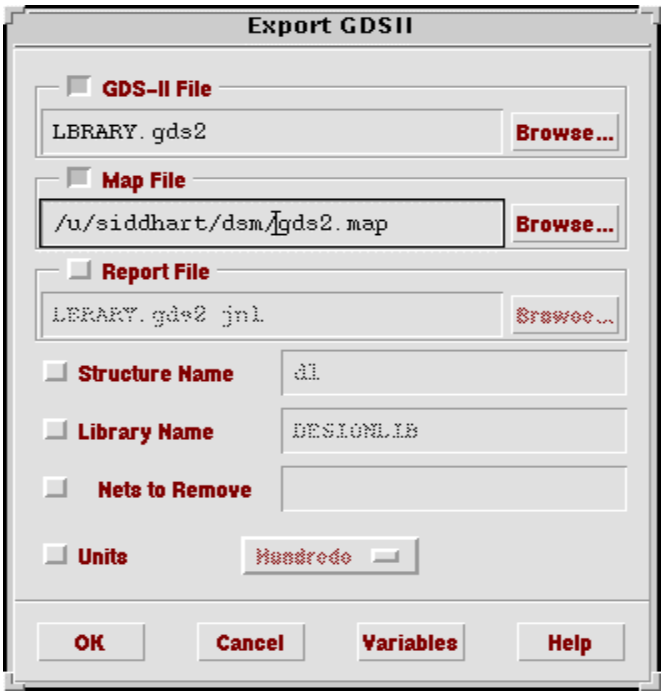

Fig 18: Exporting Design

Importing the Design in Cadence:

Start Cadence by typing the following command in the command prompt.
hostname.ece.pdx.edu> icfb &

In CIW window
Click on ***File -> import -> stream.*** This brings up "Virtuoso Stream In" form.
Fill the Input File name as the one exported from Silicon Ensemble with extension.gds2 (e.g. *LBRARY.gds2*).
Fill the **Top Cell Name** as your design name (e.g. *dl*).
Fill the **Library Name** with your library name (e.g. *cell*) as shown in Fig 19.

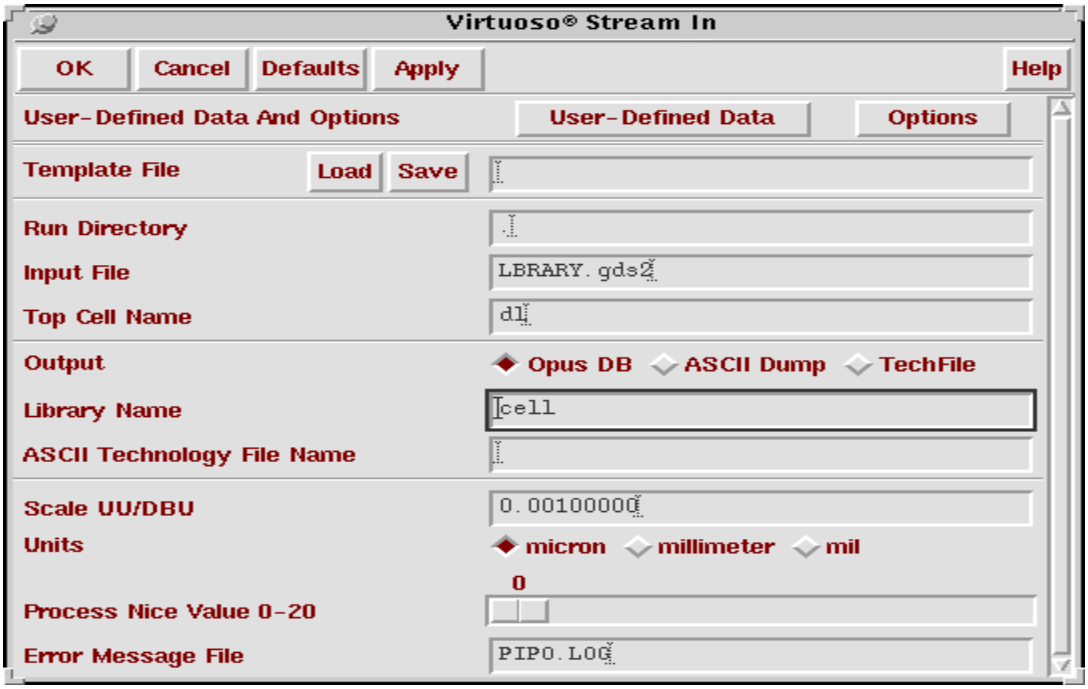

Fig 19: Virtuoso Stream In

Click ***Options*** tab on the "Virtuoso Stream In" form .This brings up "Stream In Options" form. Click ***Snap XY to Grid Resolution*** and***Retain Reference Library (No Merge)*** as shown in Fig 20.
Click ***OK***.

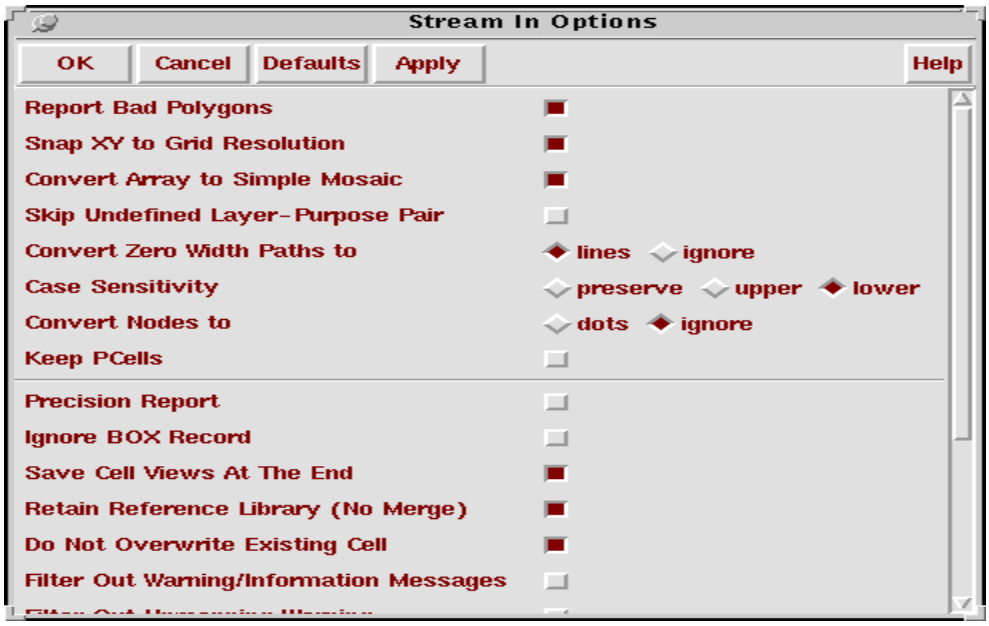

Fig 20: Stream In Options

Click ***OK***.

Now the GDS2 file has been imported in cadence.
Open your top cell layout (e.g. dl).The layout should appear as shown in Fig 21.

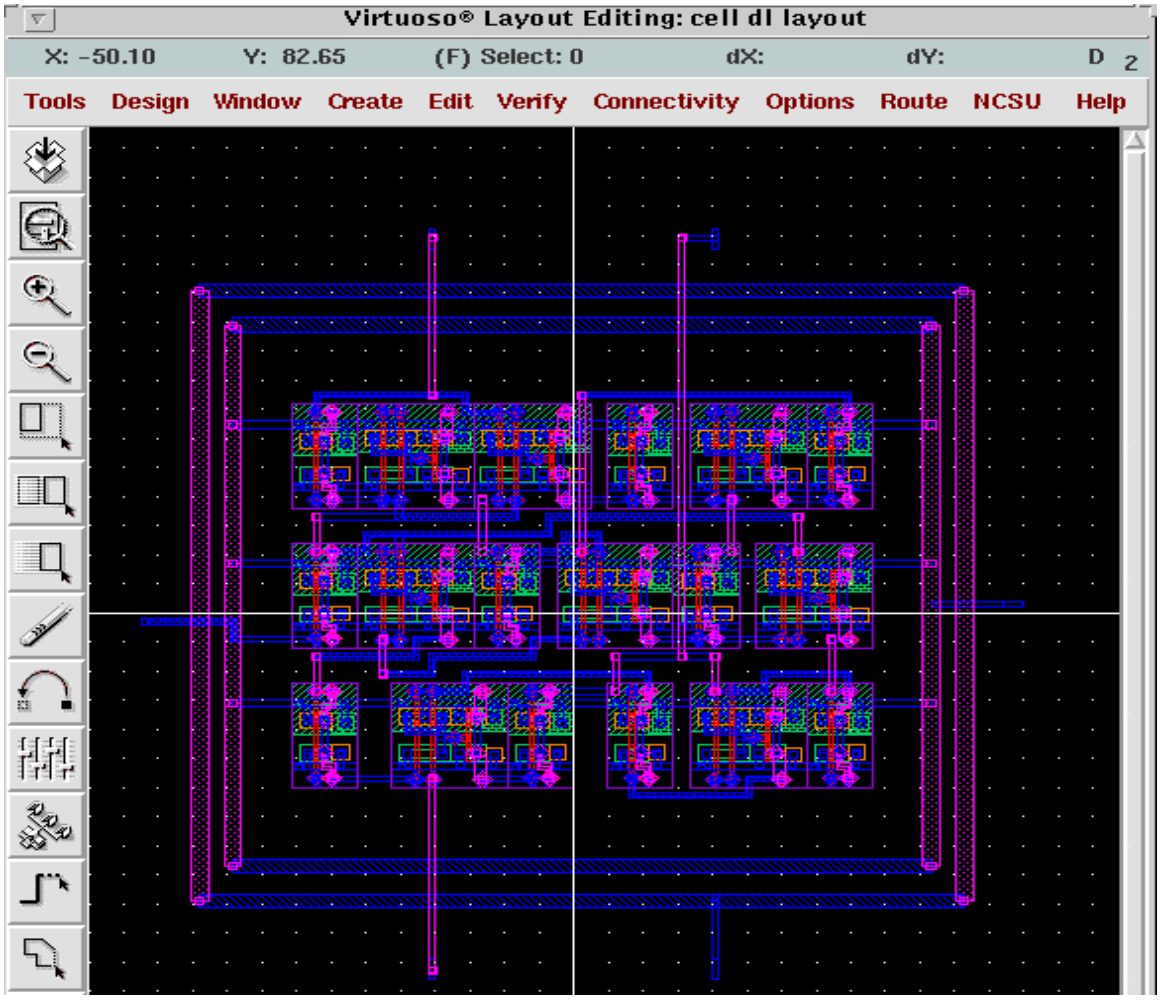

Fig 21: Layout view

Create pins from labels:

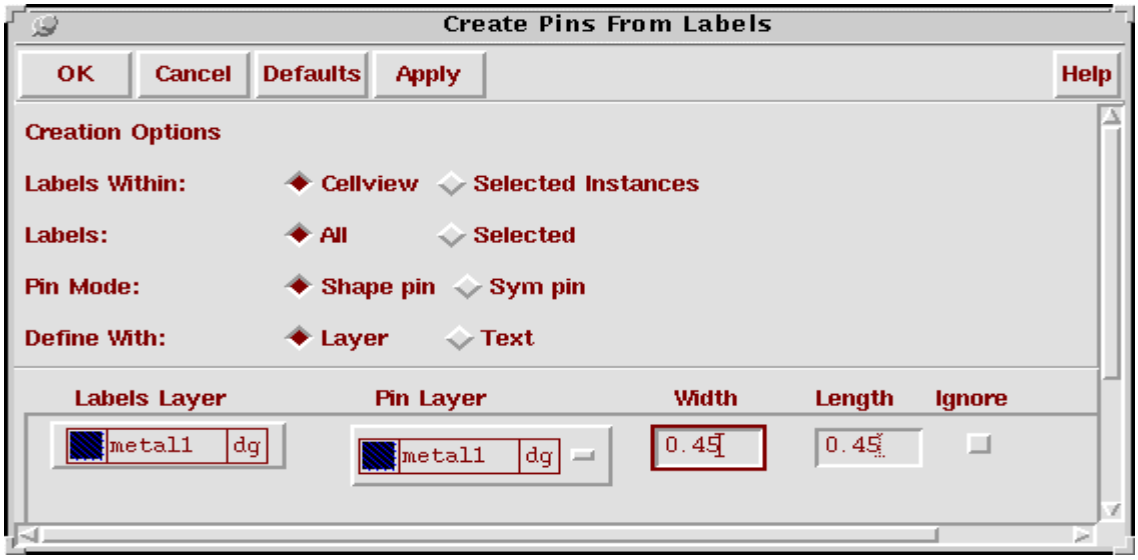

Fig 22: Create Pins From Labels

1. When you export the routed layout from the silicon ensemble to the virtuoso in the GDS-11 format all the pin labels are in the metal1 dg.
2. Change the layer of the labels from metal1 to *text drawing*.
3. The connectivity of all the pins in the layout is input-output. So change the connectivity of the pins according to the schematic.
4. Add gdd! and gnd! pins manually to the power and ground rails of the generated layout.
5. Now you can perform DRC and LVS on your design.