Silicon Ensemble using
DEF FileTutorial 5
Release Date: 01/13/2005(Version 2)AUTOMATIC PLACE AND ROUTE IN SILICON ENSEMBLE
USING DEF

Type the following command to invoke the tool. *hostname.ece.pdx.edu> sedsm -m \&* The "Silicon Ensemble" window should appear as shown in Fig1.

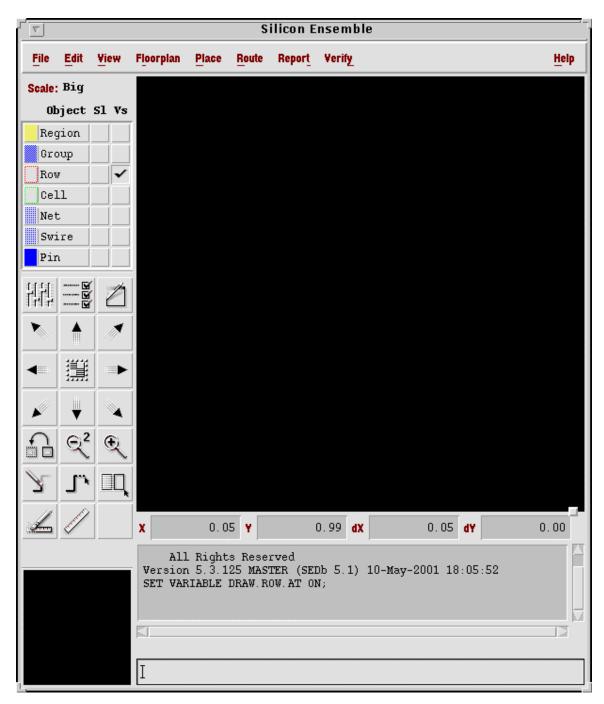


Fig 1: Silicon Ensemble Window

- 1 -

Click on *File -> Import -> LEF* in the "Silicon Ensemble" window .This brings up the "Import LEF" form as shown in Fig 2. Select the .lef file and import it as shown in Fig 2.

Filter	
*.lef	
Directory and File List	
<pre>[Up one directory] .abstract/ .hld/ STD.lef amit1.lef amit2.lef amit3.lef amit3/ amit4.lef</pre>	Ê
Selection	p.s.
/u/siddhart/dsm/cell.lef	
Report File	
importlef.rpt	Browse
Options	
💷 Clear Existing Design Data 🔲 Expand Paths	B
Case Sensitive Names	

Fig 2: Import LEF

Click on *File -> Import -> DEF* in the art work window. This brings up "Import DEF" form as shown in Fig 3.Choose design directory as your path as shown in Fig 3.

Filter
*.def
Directory and File List
[Up one directory] .abstract/ .hld/ 123.def LBRARY.def amit3/def amit3/ cds_vbin/ insl.def man.def p.def
Selection
/u/siddhart/dl1.def
Options Allow EEQ Substitutions Report File
LBRARY. importdef. rpt Browse OK Apply Cancel Variables Help

Fig 3: Import DEF

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Initialize Floorplan:

Click on *Floorplan-> Initialize Floorplan*. This brings up "Initialize Floorplan" form. Fill the form as shown in Fig 4.

Init	ialize Floorplan		
Design Statistics Number of: Cells 18 Blocks 0 IO Pads 0 IO Pins 0 Corner Pads 0 Nets 22 Area (Square Microns) Cells 4147.20	Die Size Constraint Aspect Ratio Height Width Fixed Size	AspectRatio	1.0
IO To Core Distance Left / Right microns 20.00 Top/Bottom microns 20.00	Core Area Parameters Row Utilization(%) Row Spacing Block Halo Per Side I Flip Every Other Row	microns 🖃	70 [°] , 0 4 [°] , 00 20.00 Abut Rows
Calculate Expected Results Aspect Ratio: 1.00 Width: 123.12 micro: Core row utilization = 92.40%. Chip Area = 15158.53 sq. microns. I0 to Core Distance (microns): X: 20.0 Number of Standard Cell Rows = 3. Design is core-limited.		ons.	

Fig 4: Initialize Floorplan

Fill the **IO To Core Distance** as 20 microns both for **Top/ Bottom** and **Left / Right**. Fill the **Row Spacing** to 4 to 5 microns.

For **Row Utilization** (%) starting from 80% and run placement (PLACE Cells). If the cells are placed then its fine otherwise repeat the step by decreasing the value of row utilization. The floorplan will appear in the Silicon Ensemble window as shown in Fig 5

Silicon	n Ens	semble	e using			Tutor	ial 5					-
	DEF	File	-		Re	lease D	ate: (01/1	13/2005(Versi	ion 1	2)	
∇						LBI	RARY	•			, 	
File	Edit	¥iew	Floorplan	Place	Route	Report	Verif	Ł				Help
Scale:	Smal]	L										
Ob ;	ject	Sl Vs										
Reg												
Grov	-	~										
Cel		~										
Net												
Swi	re	~										
Pin												
퉡		Ź										
	讕											
	₩]	
6	Q2	¢										
Y	٦r											
	Į				_							
			x	-60.2	8 Y	75	5.57	dX	-10.56	dY	30.44	Sel

Fig 5: Rows after Floorplanning

ADD IO PINS:

The pins are added as the schematic of the design contains the logical pins.

In the Art work window click on EDIT -> Add -> Pin. This brings up "Add Pin" form. In the form fill as follows.

Select **NET TYPE** as **Special** for all vdd! and gnd! Pins.

Select **NET TYPE** as **Regular** for all other pins.

Select Use as **Power** for vdd! and Dir **INPUT**.

Select Use as Ground for gnd! And Dir INPUT.

Select Use as **Signal** for all input pins and Dir **INPUT**

Select Use as Signal for all output pins and Dir OUTPUT.

Write the name of pin (e.g. *vdd!*) in the Net Name and others entries as mentioned above. Click on pick and then point and then click within the boundary of the Silicon Ensemble window .Then click **OK** .Complete this for all the pins.

Silicon Ensemble using			orial 5		
DEF File		Release I	Date: 01/13	/2005(Vers	(10n 2)
-		Add	l Pin		T
	Net Name	vdd!		Pick	
	Width			0.00	
	SNAP		NET TYPE		
	🗢 ON		🔷 Regular		
	🔷 OFF		🗢 Special		
	Point				
	X1			-61.21	
	¥1			13.46	
	Layer	ver 🖃 Dir		-	
			÷		-
Į	ок	Ca	ncel	Help	

Fig 6: Add Pin Edit property Global Signal pins vdd! and gnd!:

Edit the properties of the special nets as they are routed through abutment so change their shape to abutment .To chance the properties click on the pin object on the window and then click on the vdd! and gnd! pins on the routed view. Then hit ctrl + q together .The "Edit Properties" form appears as follows. Change the shape from NORMAL to ABUTMENT as shown in Fig 7.

Name	Туре	Value	
RESISTANCE	REAL	0	A
RISESATCUR	REAL	0	
RISESATT1	REAL	0	
RISET0	REAL	0	
RISETHRESH	REAL	0	
SCANUSE	STRING	NONE	
SHAPE	STRING	[ABUTMENT	V
SPECIAL	BOOLEAN	TRUE	
TECHNOLOGY	STRING	ACTIVE	
TIEOFFR	REAL	0	2
ange: None.	ion		Pin 1 of

Fig 7: Edit Properties

- 5 -

In the Silicon Ensemble window click *Place -> IO*. Choose Random and Evenly space as shown in Fig 8.

	Place IO	
Placement Mode		
🔶 Random		
◇ I/O Constraint File	oplace.ioe Write E	dik
\diamond Refine Pin Placement	keep piez on zame zide	
— 🔜 Pin Layer Assignme Top / Bottom	nt metaiz 💴	
Loff / Right		
Space : 🔶 Evenly 🔷	Abutted 🔷 Center Abutted	
OK	Cancel He	ID

Fig 8: Place IO

Place Cells:

Choose Place Cells in the SE window. This brings up "Place Cells" form . In the form click *OK*.

🔟 Timing Driven Plac	ement		
💷 Power Driven Plac	ement		
🗐 Timing Analysis	Report File		
🗐 Pin Placement			
🔲 Generate Congesti	on Man		
Optimize :	•		
Timing Signal	l Integrity 🔲	Scan Chains	
Options		LERARY, goopt.	rpt

Fig 9: Place Cells

This will place the cells as shown in Fig 10.

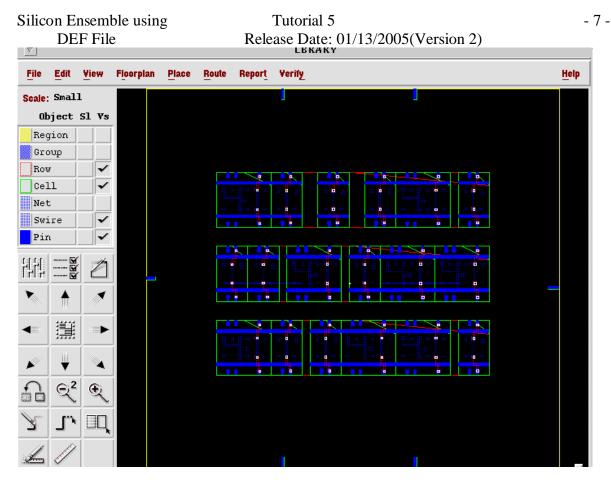


Fig 10: IO Pins and Cells Placed

Power Routing:

Click on *Route ->Plan Power*

Click on Add Rings as shown in Fig 11.



Fig 11: Plan Power (PP)

Nets "vdd!"	" "gnd!"				
Ring	Layer	Core Ring Width	Core Ring Space	ng	Block Ring Widt
Horizontal	metal1 💷	3. Ğ <u>0</u>	Center 💷	0 00	0.00
Vertical	metal2 💷	3.60	Center 💷 🛛	0 00	0.00
Netx					
Netz Ning	Layer	Core Ring Width	Core Ring Space	9	Black Ring Width
	Layer	Care Ring Width	Core Ring Spanin	9	Slock Ring Width

Fig 12: PP Add Rings

The Silicon Ensemble window appears as follows (Fig 13).

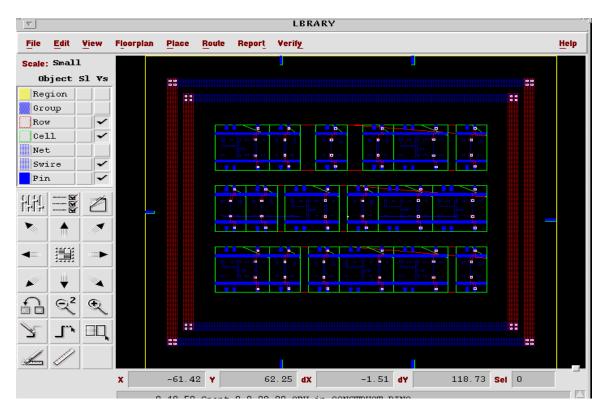


Fig 13: Cells with Power and Ground Rings

Then Click on *Route-> Connect Ring*. This brings up the "Connect Ring" form. Make sure you have vdd! and gnd! in the Nets as shown in Fig 14. Leave all settings as default .Click *OK*.

Connect Ring						
Nets "vdd!" "gnd!"						
Туре						
🔲 Stripe						
🗏 Block 📃 All Ports	🔲 Maximum Width	0.00				
	Selected Blocks					
🗖 IO Pad 💦 🗖 All Ports	🗐 Maximum Width	0.00				
🔲 IO Ring	🗐 Pin Width	0.00				
Follow Pins	🗐 Pin Width	0.00				
OK Apply Ca	ancel Variables	Help				

Fig 14: Connect Ring

The Silicon Ensemble window appears as shown in Fig 15.

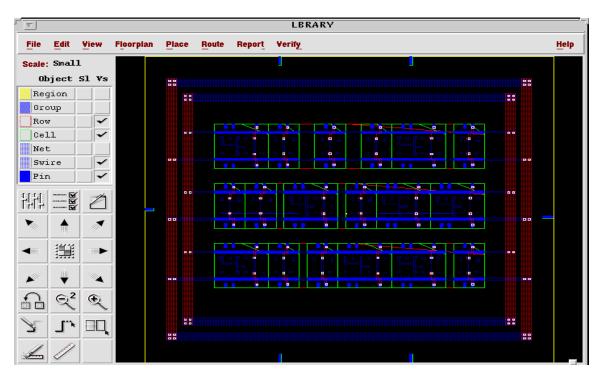


Fig 15: Cells with connected Rings

Silicon Ensemble using DEF File Signal Routing:

In the Silicon Ensemble window click *Route -> Wroute*. This brings up the Make sure that both **Global and Final Route** and **Auto Search And Repair** are enabled. Click *OK*.

WRoute
Routing Mode
Global and Final Route Auto Search And Repair
♦ Incremental Final Route ☐ Rodo Global Naule for visiatione
Timing Driven Routing
OK Cancel Options Variables Help

Fig 16: WRoute

Silicon Ensemble window appears as shown in Fig 17.

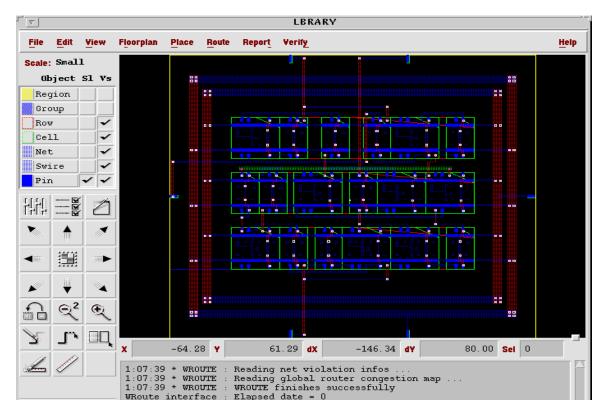


Fig 17: Cells after signal routing

Silicon Ensemble using
DEF FileTutorial 5
Release Date: 01/13/2005(Version 2)Exporting the Design:In the Silicon Ensemble window click *File -> Export -> GDSII*.Enable GDS-II File and fill the section with a file name with extension .gds2 (e.g.
LBRARY.gds2).Enable Map File and give it path
/home/ece/username/dsm/gds2.map
as shown in Fig 18.

Click OK.

E	Export GDSII			
🗖 🗖 GDS-II File —				
LBRARY. gds2		Browse		
Map File				
/u/siddhart/dsm	Browse			
Report File				
LERARY.gds2 jn)	LERARY. gds2 jnl			
Structure Name	d1.			
🔲 Library Name	DESIGNLIB			
Nets to Remove				
🗆 Units	Hundredo 💷			
OK Can	cel Variables	Help		

Fig 18: Exporting Design

Importing the Design in Cadence:

Start Cadence by typing the following command in the command prompt. *hostname.ece.pdx.edu> icfb* &

In CIW window Click on *File -> import -> stream*. This brings up "Virtuoso Stream In" form. Fill the Input File name as the one exported from Silicon Ensemble with extension.gds2 (e.g. *LBRARY.gds2*). Fill the **Top Cell Name** as your design name (e.g. *dl*). Fill the **Library Name** with your library name (e.g. *cell*) as shown in Fig 19.

r 🖉			Vi	rtuoso® Stream In	
ок	Cancel	Defaults	Apply		Help
User-Det	fined Data	And Optio	ns	User-Defined Data Options	IA
Template	File	Load	Save	Tree control of the second sec	
Run Direc	ctory			, in the second s	_
Input File				LBRARY. gdsŽ	
Top Cell I	Name			dl	
Output				🔶 Opus DB 🐟 ASCII Dump 🐟 TechFile	
Library N	lame			Icell	
ASCII Te	chnology A	File Name		,	
Scale UU	/DBU			0.00100000	
Units				ightarrow micron $ ightarrow$ millimeter $ ightarrow$ mil	
Process	Nice Value	0-20		0	
Error Me	ssage File			PIPO.LOC	

Fig 19: Virtuoso Stream In

Click *Options* tab on the "Virtuoso Stream In" form .This brings up "Stream In Options" form. Click *Snap XY to Grid Resolution* and *Retain Reference Library (No Merge)* as shown in Fig 20. Click *OK*.

_			Strea	m In Options	
ок	Cancel	Defaults	Apply	He	qle
Report B	ad Polygo	ns		—	A
Snap XY	to Grid Re	esolution		-	Ш
Convert /	Array to S	imple Mosa	aic	—	Ш
Skip Und	efined Lay	er-Purpos	e Pair		Ш
Convert 2	Zero Width	Paths to		🗢 lines 🐟 ignore	Ш
Case Ser	sitivity			🔷 preserve 🐟 upper 🔶 lower	Ш
Convert	Nodes to			🔷 dots 🗢 ignore	Ш
Кеер РСс	ells			_	
Precision	Report				
Ignore B	OX Record	l i i i i i i i i i i i i i i i i i i i			
Save Cel	l Views At	The End		—	
Retain Re	eference L	ibrary (No	Merge)	—	
Do Not O	verwrite	Existing Ce		—	
Filter Out	t Warning/	Information	Messag	es 🔟	
Ellen Out					17

Fig 20: Stream In Options

Click OK.

IC Design and Test Laboratory

Silicon Ensemble using DEF File

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Now the GDS2 file has been imported in cadence.

Open your top cell layout (e.g. dl). The layout should appear as shown in Fig 21.

$\overline{\nabla}$			Virtu	oso®	Layout	Editing	cello	il layout				1-
X: -:	50.10	Y: 82	.65	(F) 3	Select: ()	d×	t:	dY:		D 2	2
Tools	Design	Window	Create	Edit	Verify	Connec	tivity	Options	Route	NCSU	Help	
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Ā					· ·							
Q					· · ·							
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5												

Fig 21: Layout view

Create pins from labels:

9			Cre	ate Pins F	rom Labels			
ок	Cancel	Defaults	Apply					Help
Creation	Options							A
Labels Wi	ithin:	🔶 Cellv	iew 💠 S	elected Ins	tances			
Labels:		🔶 All	⇔ s	elected				
Pin Mode	:	🔶 🔶 Shap	e pin 💠	Sym pin				
Define Wi	ith:	🔶 Laye	r 💠 1	Text				
Label	ls Layer		Pin Layer		Width	Length	Ignore	
me	etall d	g 🛛	metal1	dg 🗖	0.45	0.45		
								V

Fig 22: Create Pins From Labels

- 1. When you export the routed layout from the silicon ensemble to the virtuoso in the GDS-11 format all the pin labels are in the metall dg.
- 2. Change the layer of the labels from metal1 to *text drawing*.
- 3. The connectivity of all the pins in the layout is input-output. So change the connectivity of the pins according to the schematic.
- 4. Add gdd! and gnd! pins manually to the power and ground rails of the generated layout.
- 5. Now you can perform DRC and LVS on your design.

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