Standard Cell based Automatic placing and routing using Verilog netlist in Silicon Ensemble:

Files needed for automatic placement and routing in silicon ensemble:

1. LEF file created using Abstract Generator.
2. Verilog netlists for all the schematics right from the top hierarchical design to all the standard cells.

1. Start Silicon Ensemble:

Start the silicon ensemble design environment by typing the following:

Hostname.ece.pdx.edu > sedsm –m=500

Here 500 is the memory allocated for silicon ensemble. The “Silicon Ensemble” window opens as shown in Fig 1.

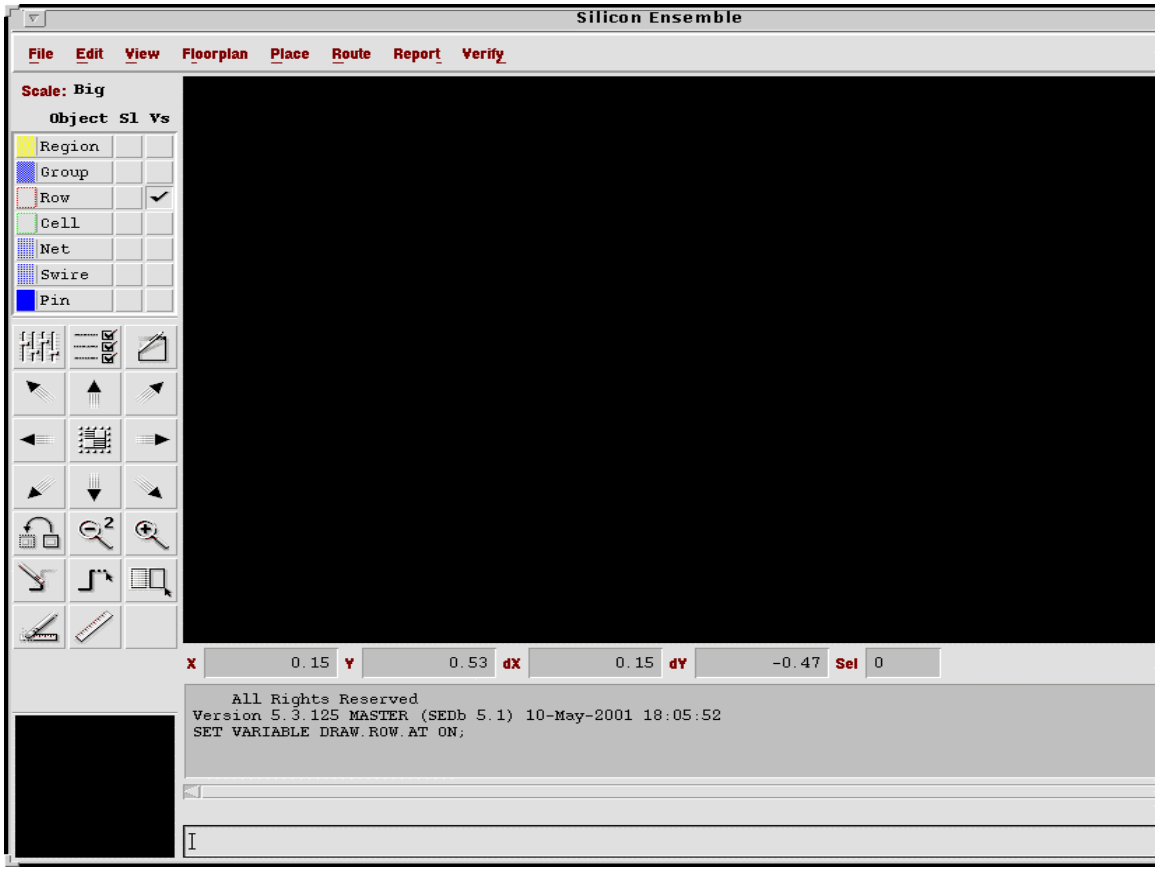

Fig 1: Silicon Ensemble

2. Import Files:

You will have to import the LEF file which is created using the Abstract generator and also the verilog netlists.

a. Importing LEF file:

1. In Fig 1 select ***File –> Import –> LEF***.

2. The “Import LEF” window opens as shown in Fig 2. Select your LEF file.
3. Also select **Clear Existing Design Data** and click ***OK*** to import the LEF file.
4. Watch the command text at the bottom of the main window to make sure there are no errors in the LEF file. You should see something like this if the .lef file was imported successfully:

   ##-I No errors found. The database created successfully.

   Thus importing of the LEF file is done.

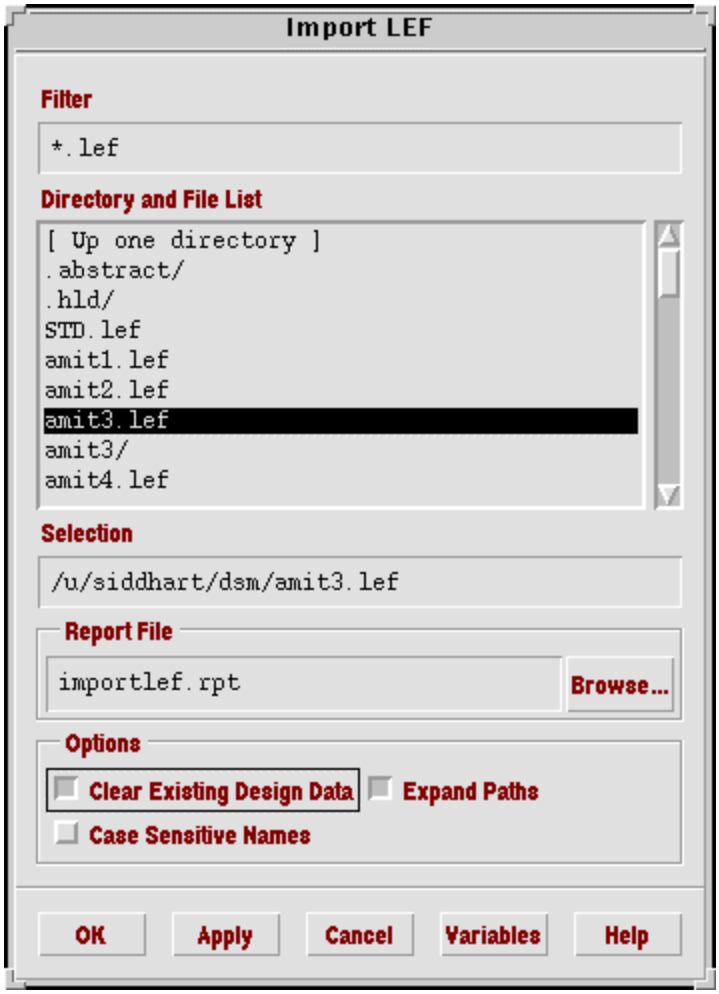

Fig 2: Import LEF

b. Importing Verilog netlist:

1. In Fig 1 select ***File –> Import –> Verilog***.

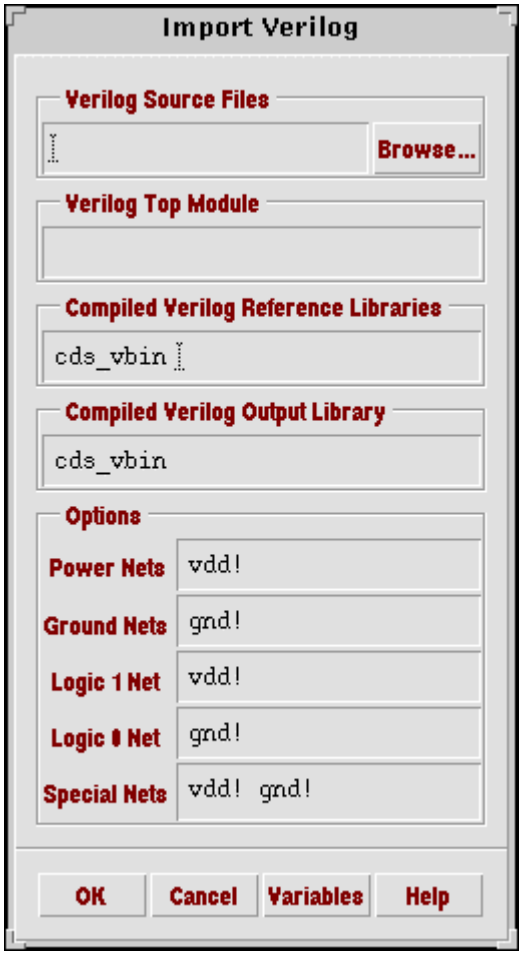

Fig 3: Import Verilog

2. The “Import Verilog” window opens as shown in Fig 3. In the **Verilog Source Files** text box select all the verilog netlists that are needed for your design. Fig 4 shows all the selected netlists.

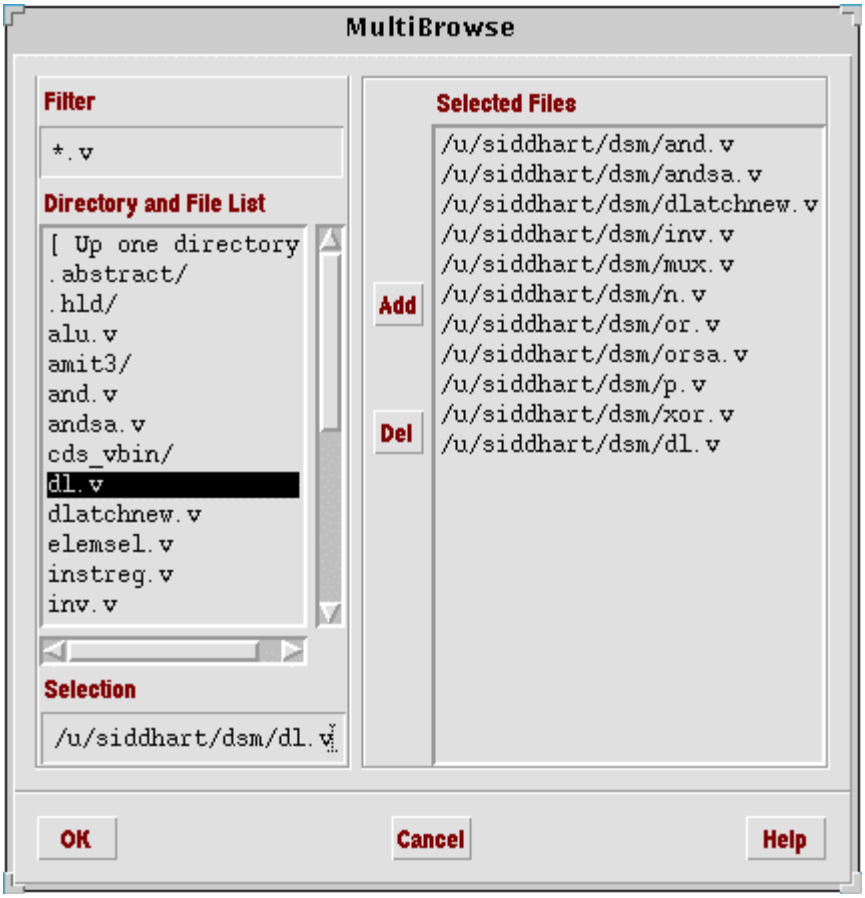

Fig 4: Selecting the Verilog netlist's

3. Click ***OK*** in Fig 4. In the "Import Verilog"(Fig 3) window enter the name of the primary module in the **Verilog Top Module** text box. This is the name of the hierarchial top module in the verilog netlist.
4. In the **Compiled Verilog Reference Libraries** text box just type *cds_vbin.*
5. Replace vdd! and gnd! with vdd and gnd for all the categories in "Import Verilog" form as shown below.

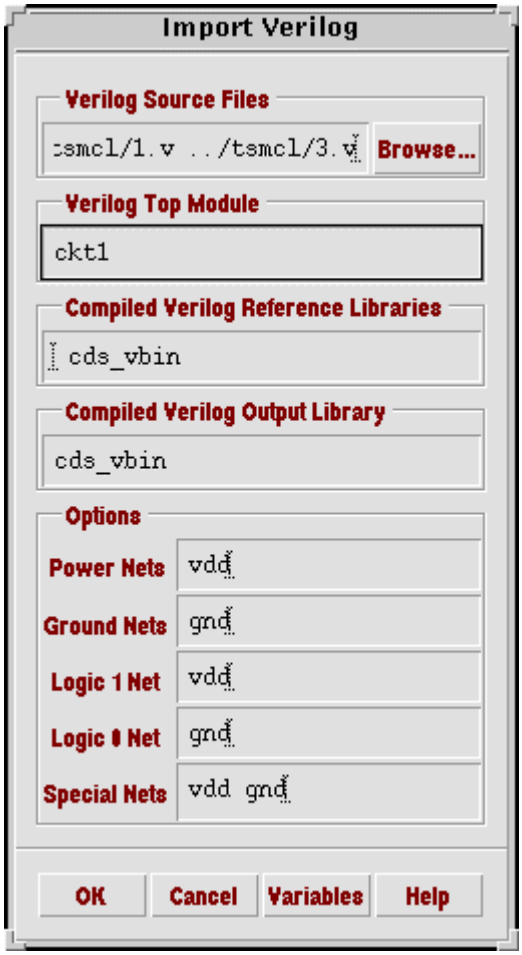

Fig 5: Completed Import Verilog form

6. After completing all these steps the form shown in Fig 3 looks as shown in Fig 5. Click ***OK***. Watch the command text box to make sure there are no errors in importing the verilog netlist. Thus importing of the verilog netlists is done.

3. **Floorplanning:**

a. In "Silicon Ensemble" window select ***Floorplan –> Initialize Floorplan*** to open the floorplanning window. The window appears as shown in Fig 6.

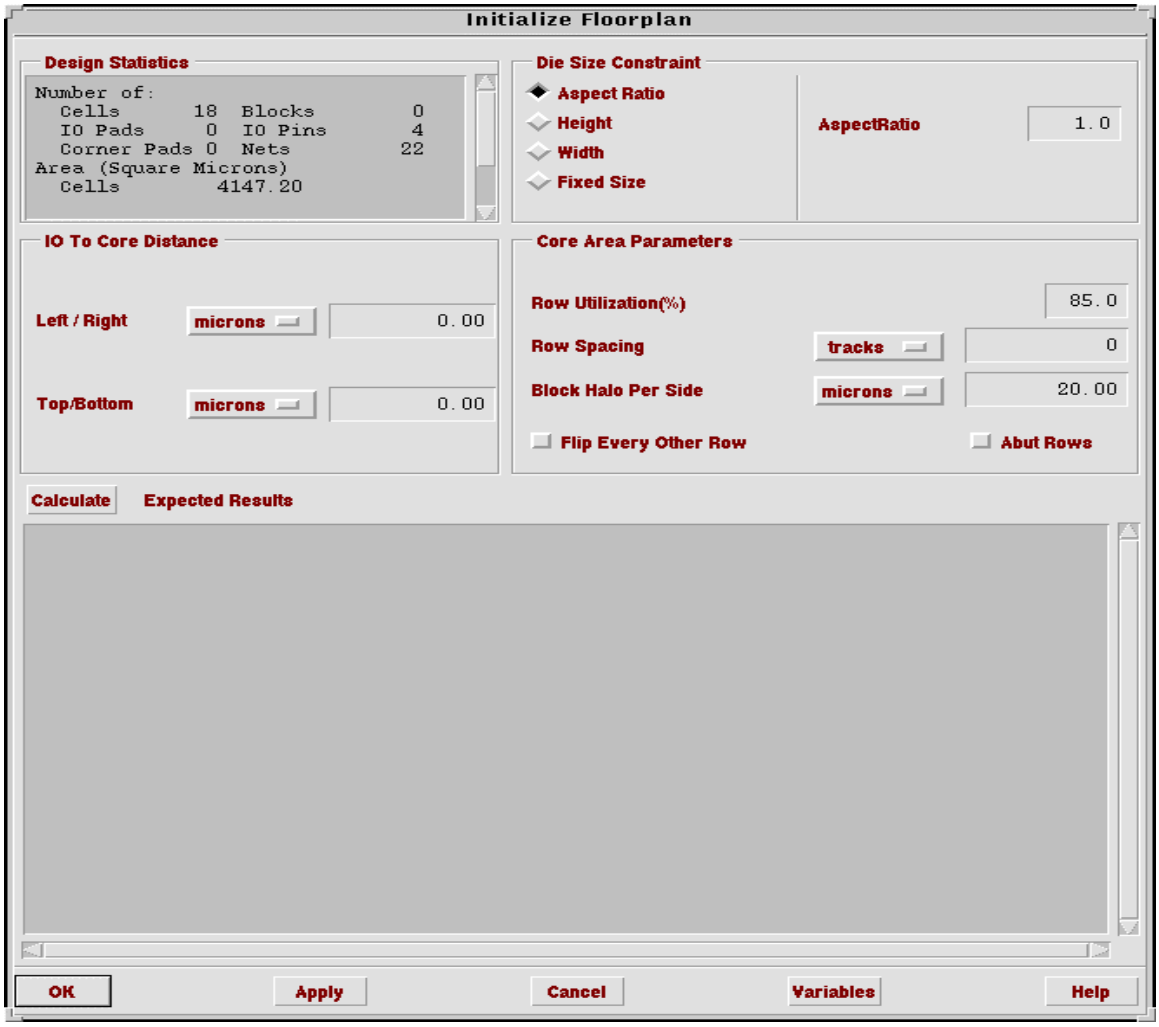

Fig 6: Initialize Floorplan

b. In **Die Size Constraint** field the **AspectRatio** is set to 1. You can change the aspect ratio to change the ratio between height and width of the design.
c. Set the **IO To Core Distance** to 20 microns for both directions. If the design has room after routing you can change this distance and rerun the whole procedure after floorplanning again.
d. In the **Core Area Parameters** the **Row Spacing** controls the distance between two rows. You can initially set this distance as 5 microns. You may reduce this afterwards to shrink the design area.
e. Set the **Block Halo Per Side** to 2 microns.
f. **Row Utilization** is set to 85% as default value.
g. Click the ***Calculate*** button to view the preliminary floorplan summary in the Expected Results text window. The “Initialize Floorplan” window now appears as shown in Fig 7.

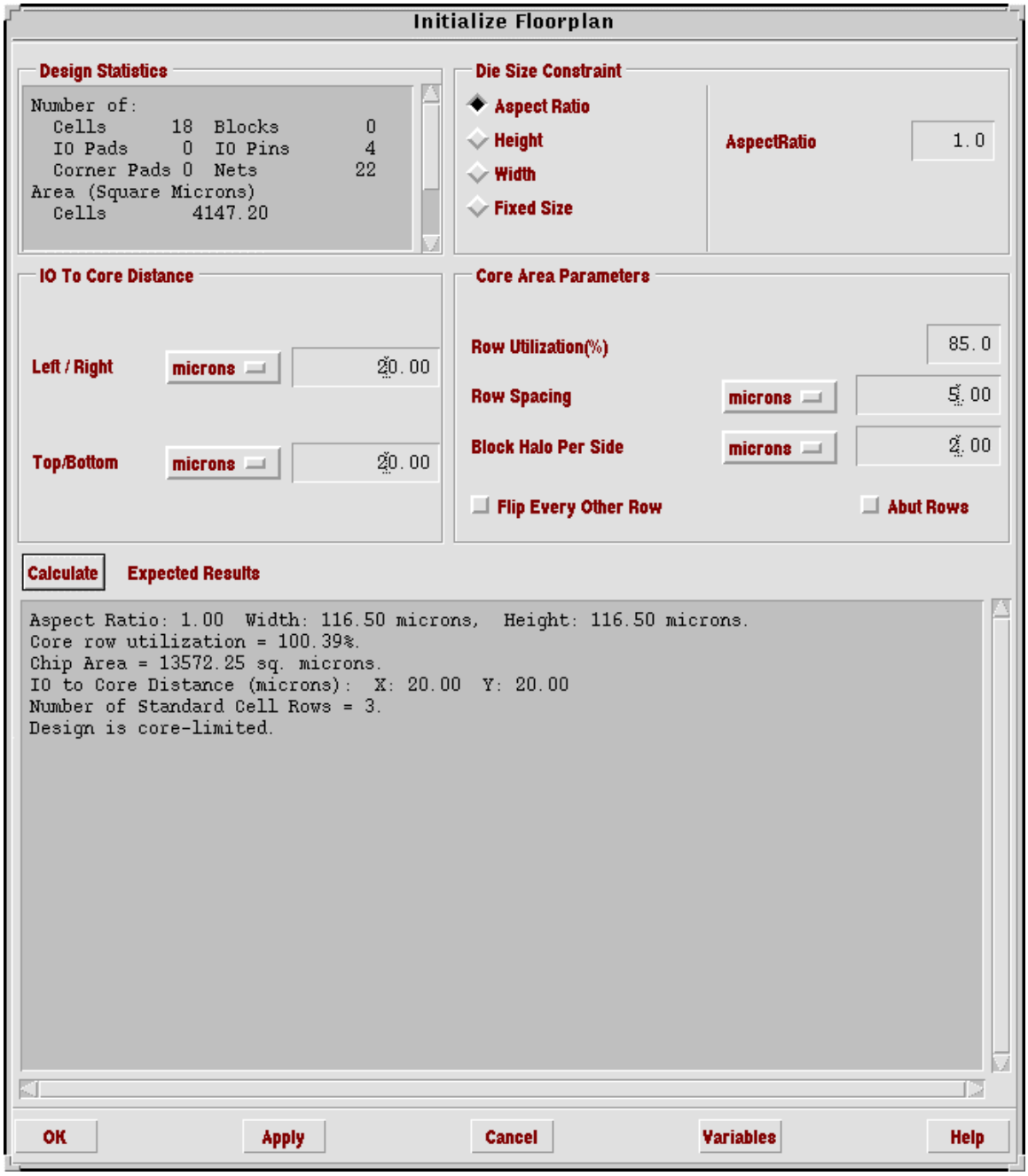

Fig 7: Initialize Floorplan

h. In Fig 7 reduce the **Row Utilization** parameter and re-calculate until the reported Core row utilization is less than 100%.
i. After the **Row Utilization** is reduced and the floorplan is recalculated the initialize floorplan window appears as shown in Fig 8.
j. In Fig 8 click ***OK*** to finalize the floorplan.

Fig 8: Final Floorplan

k. You will see the rows placed as shown in Fig 9. Thus the floorplanning is done.

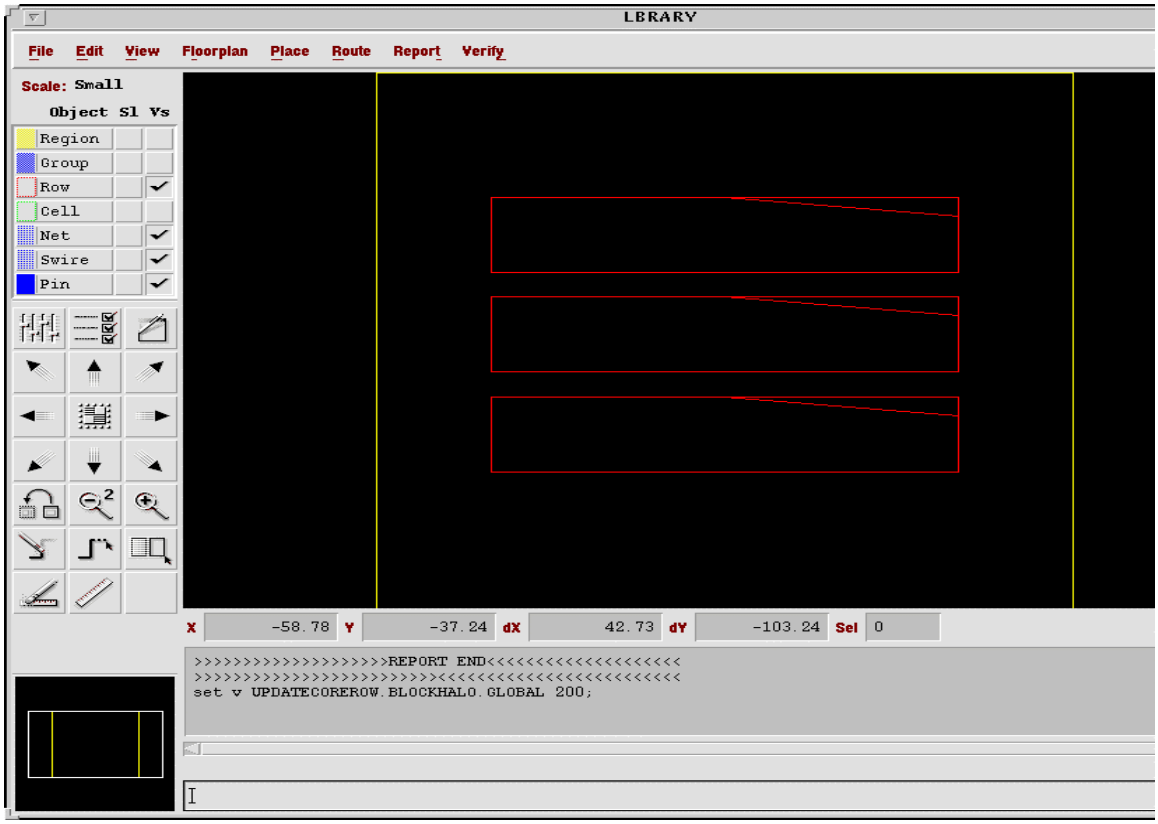

Fig 9: Rows after Floorplanning

4. Placement:

Once the floorplanning is complete, IO ports and cells need to be placed in the allotted rows.

a. In Fig 9 select ***Place –> IOs***. The "Place IO" window opens as shown in Fig 10. In Fig 10 make sure that the **Placement Mode** is set to **Random** and **Space**: **Evenly** is selected. Click ***OK***. The IOs will be placed.

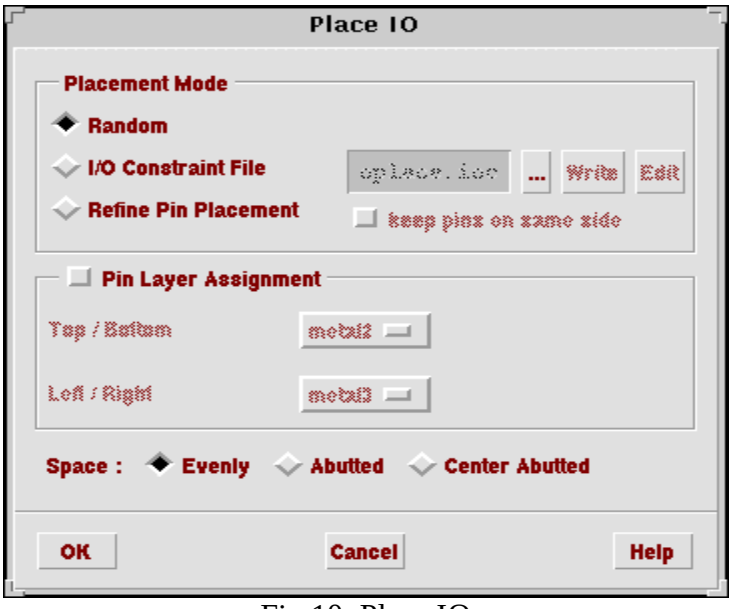

Fig 10: Place IO

The placement of the IOs is as shown in Fig 11.

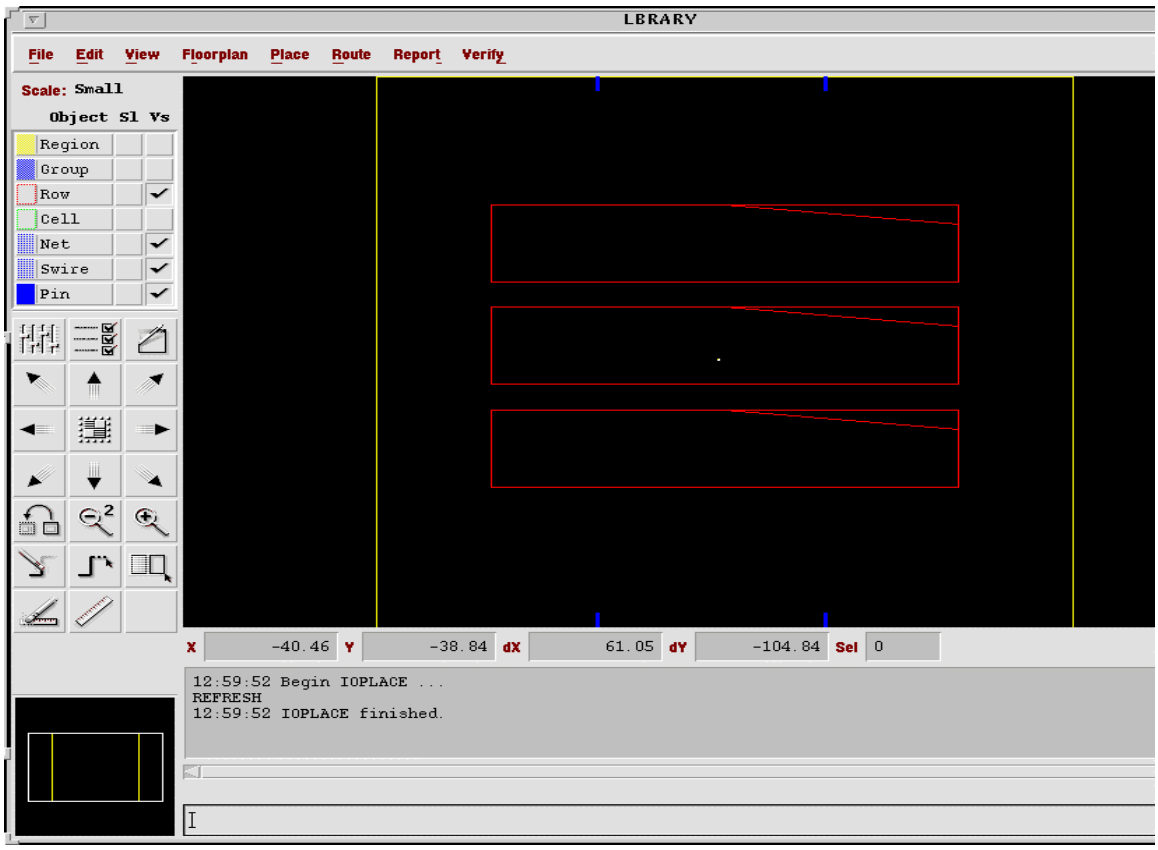

Fig 11: IOs Placed

b. In Fig 11 select ***Place –> Cells*** and the "Place Cells" window opens as shown in Fig 12. In Fig 12 click ***OK***. The cells will be placed as shown in Fig 13. If there is an error saying that Impossible to Place without Overlaps, go back to floorplanning and reduce the row utilization and repeat the procedure from floorplanning.

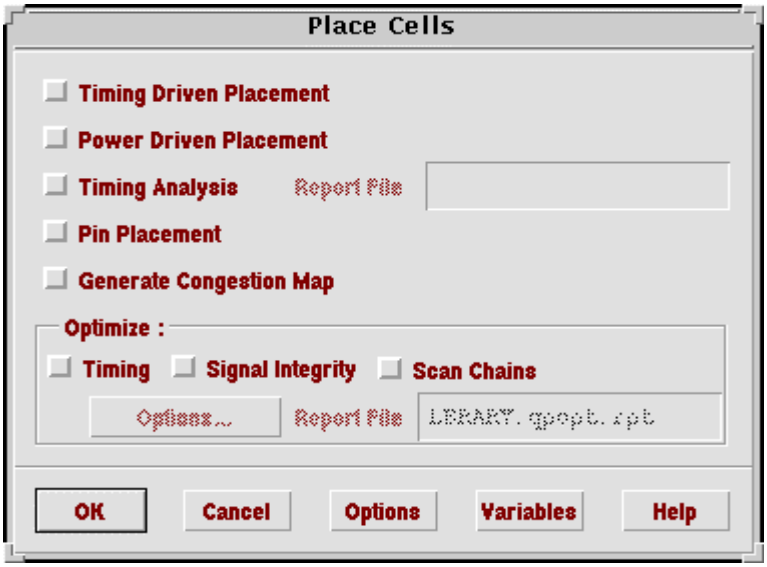

Fig 12: Place Cells

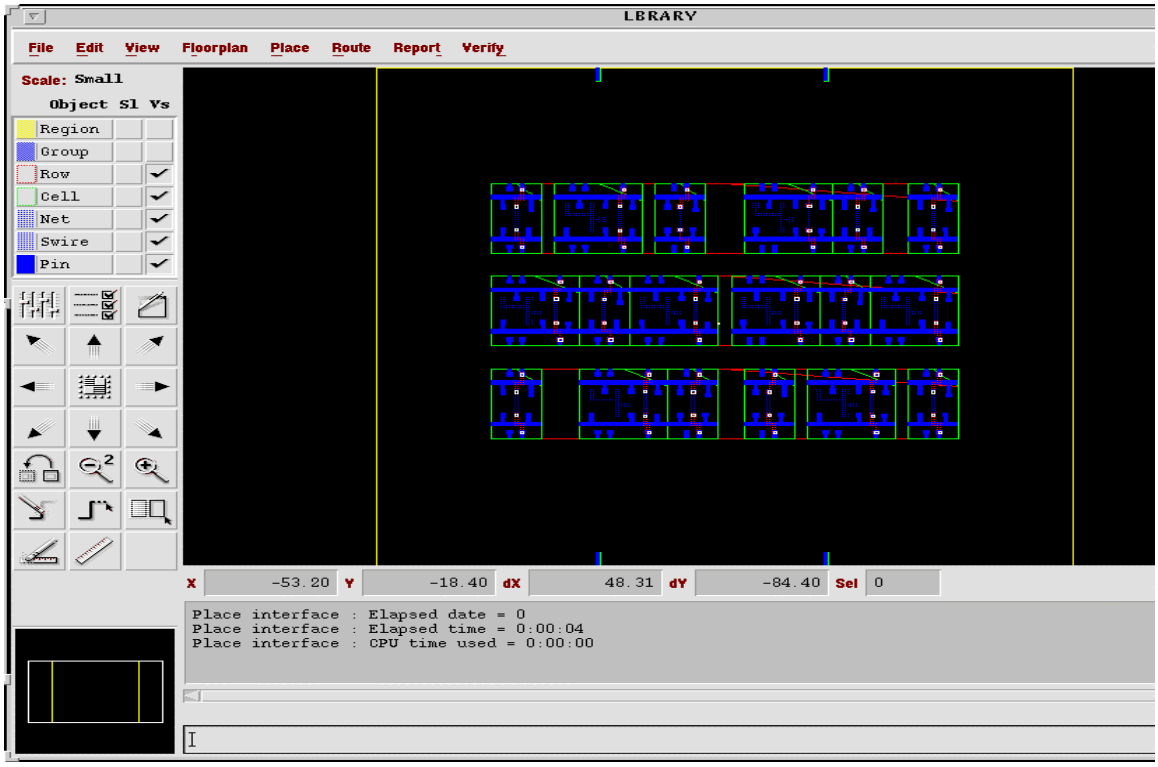

Fig 13: Cells after placing

5. Power/Ground Routing:

a. In Fig 13 select ***Route –> Plan Power*** and the "Plan Power" window opens as shown in Fig 14. In Fig 14 click ***Add Rings***.

Fig 14: Plan Power

b. The “Add Rings” window opens as shown in Fig 15. In Fig 15 set the **Core Ring Width** to 1.2 microns and click ***OK*** to apply the rings and close the “Plan Power” window. The **Core Ring width** can be set to be a multiple of 1.2. Fig 16 shows that the rings are placed.

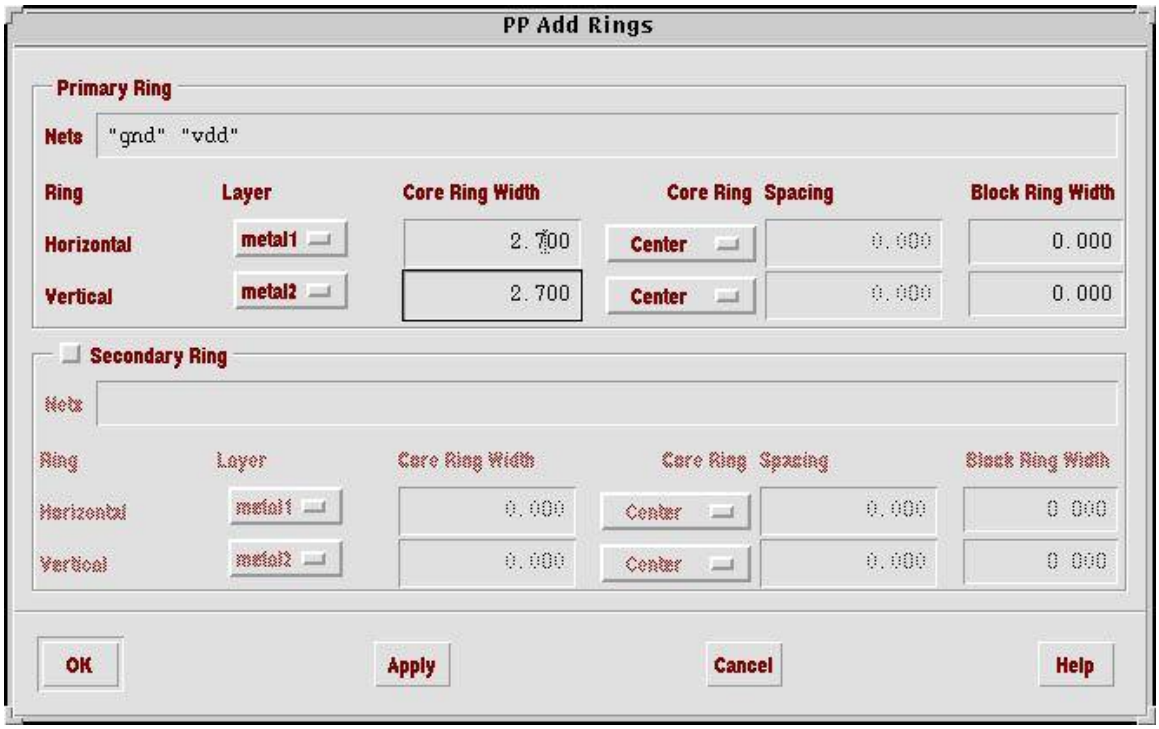

Fig 15: PP Add Rings

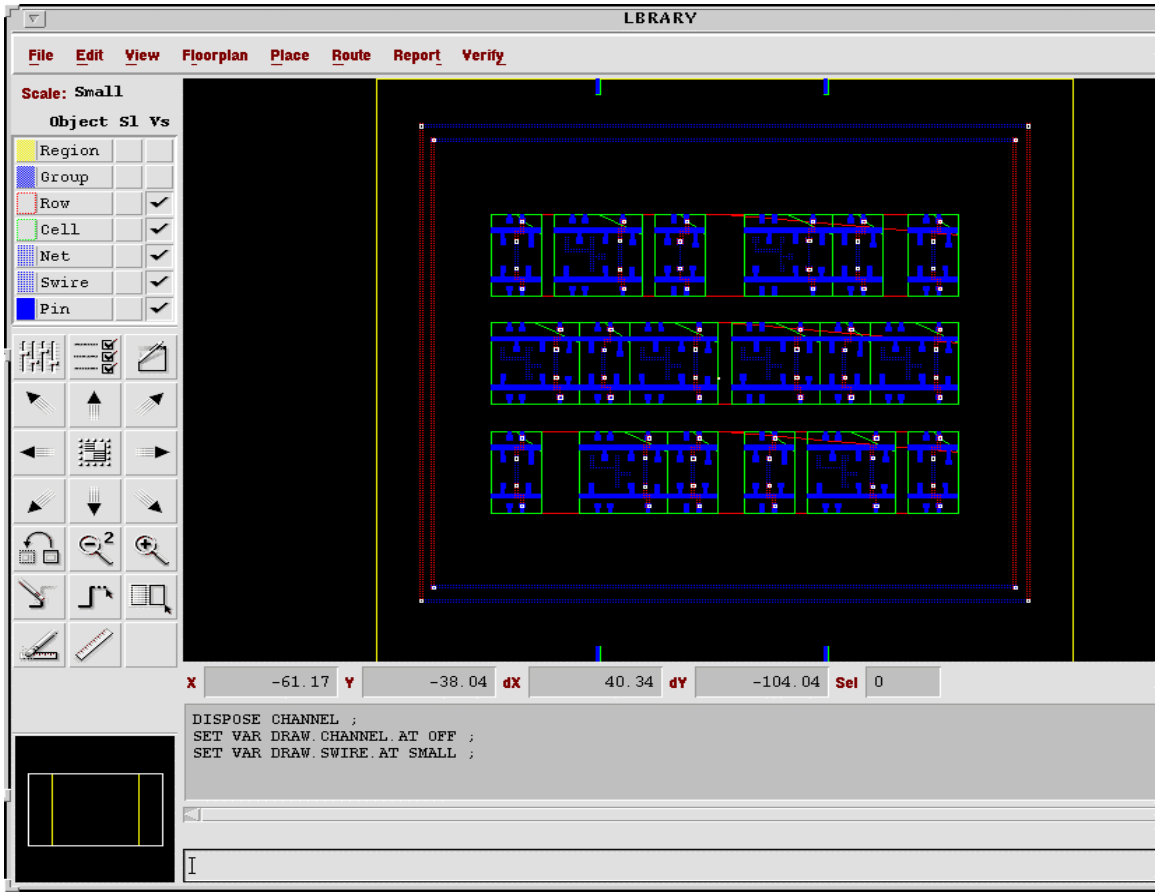

Fig 16: Cells with Rings

c. In Fig 16 select ***Route –> Connect Ring*** and the "Connect Ring" window opens as shown in Fig 17. In Fig 17 click ***OK***. This will connect your power and ground rings to your cell rows. Fig 18 shows that the cell rows are connected to the power and ground rings. Thus the Power and Ground routing is done.

Fig 17: Connect Ring

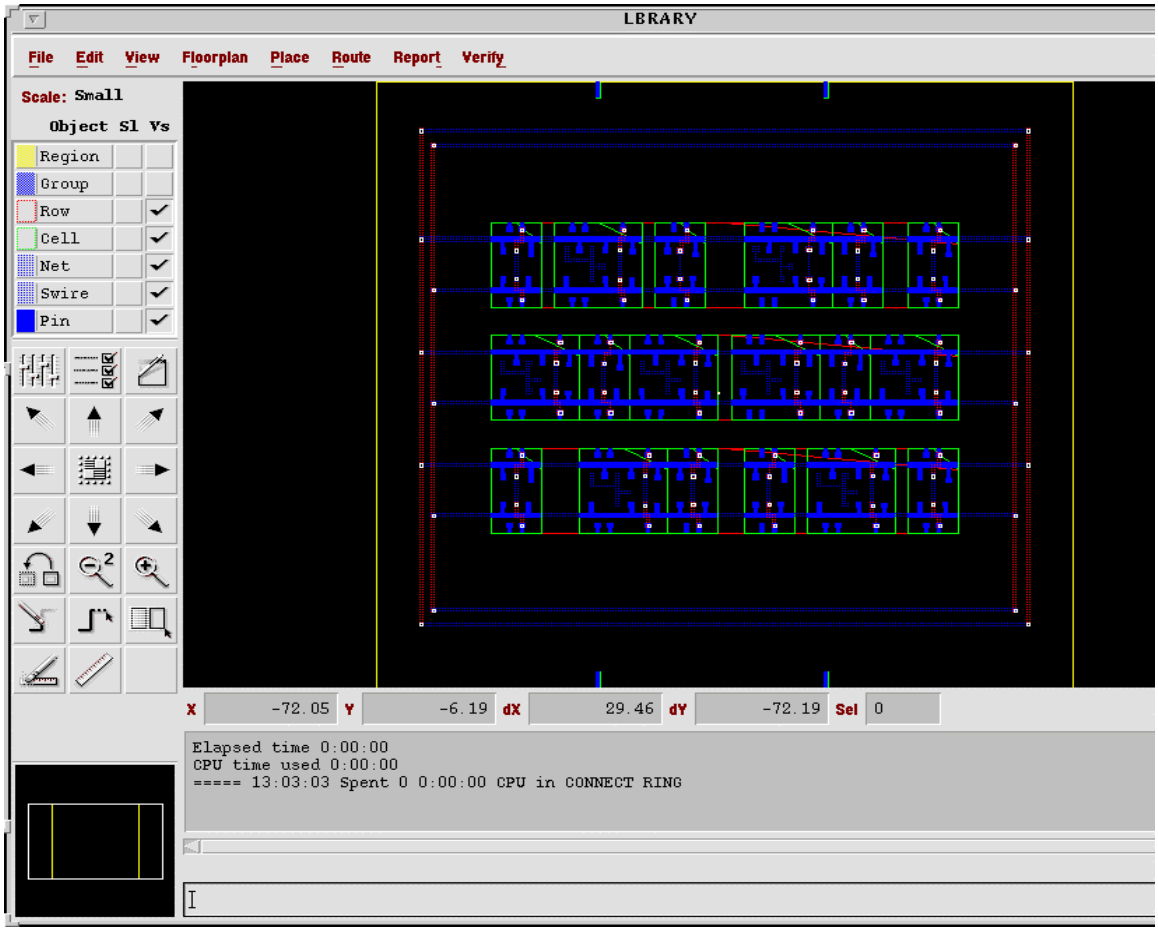

Fig 18: Rings after being connected

6. **Routing:**

a. In Fig 18 select ***Route –> WRoute***. The "WRoute" window opens as shown in Fig 19. Make sure that **Global and Final Route** and **Auto Search And Repair** are selected and click ***OK***. This will do the routing of the cells. Fig 20 shows the cells after routing.

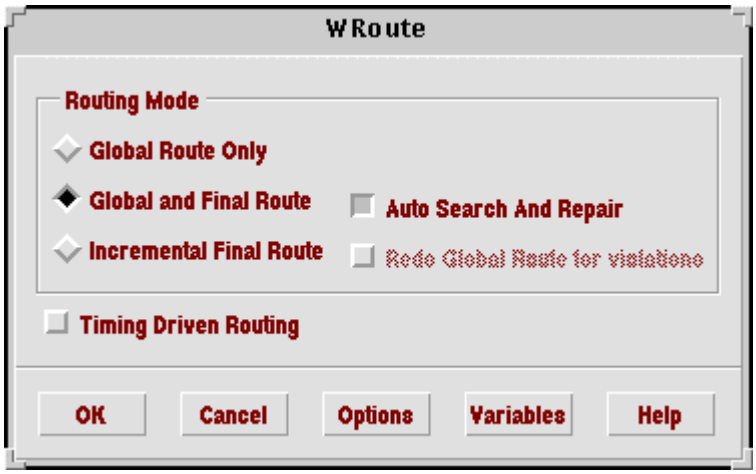

Fig 19: WRoute

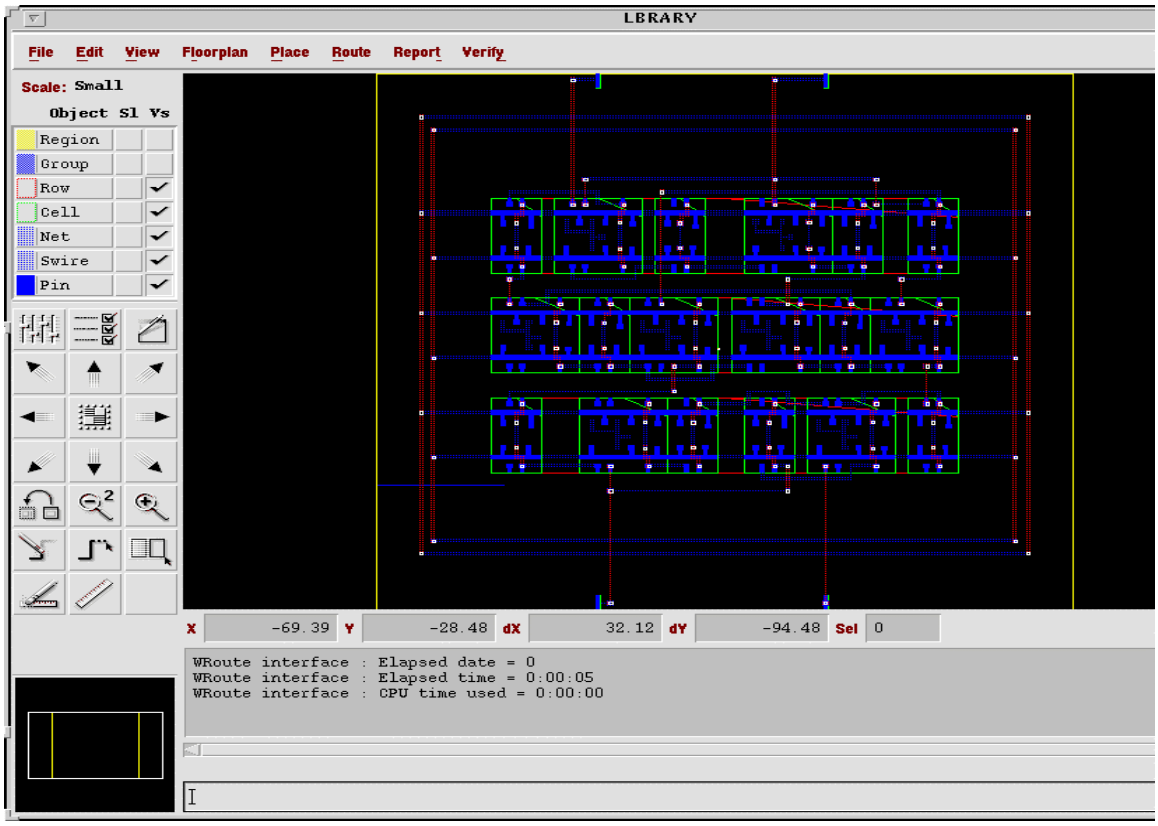

Fig 20: Cells after Routing

7. **Verify:**

a. In Fig 20 select ***Verify –> Connectivity.*** The "Verify Connectivity" window opens as shown in Fig 21. In Fig 21 click ***OK***. See to it that there are no errors or warnings in the command text window. The command text window after verifying connectivity is shown in Fig 22.

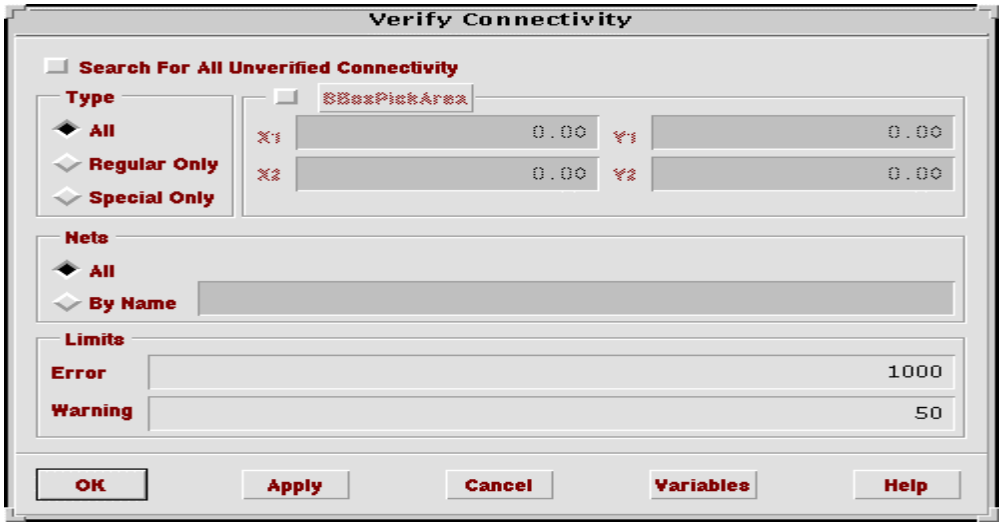

Fig 21: Verify Connectivity

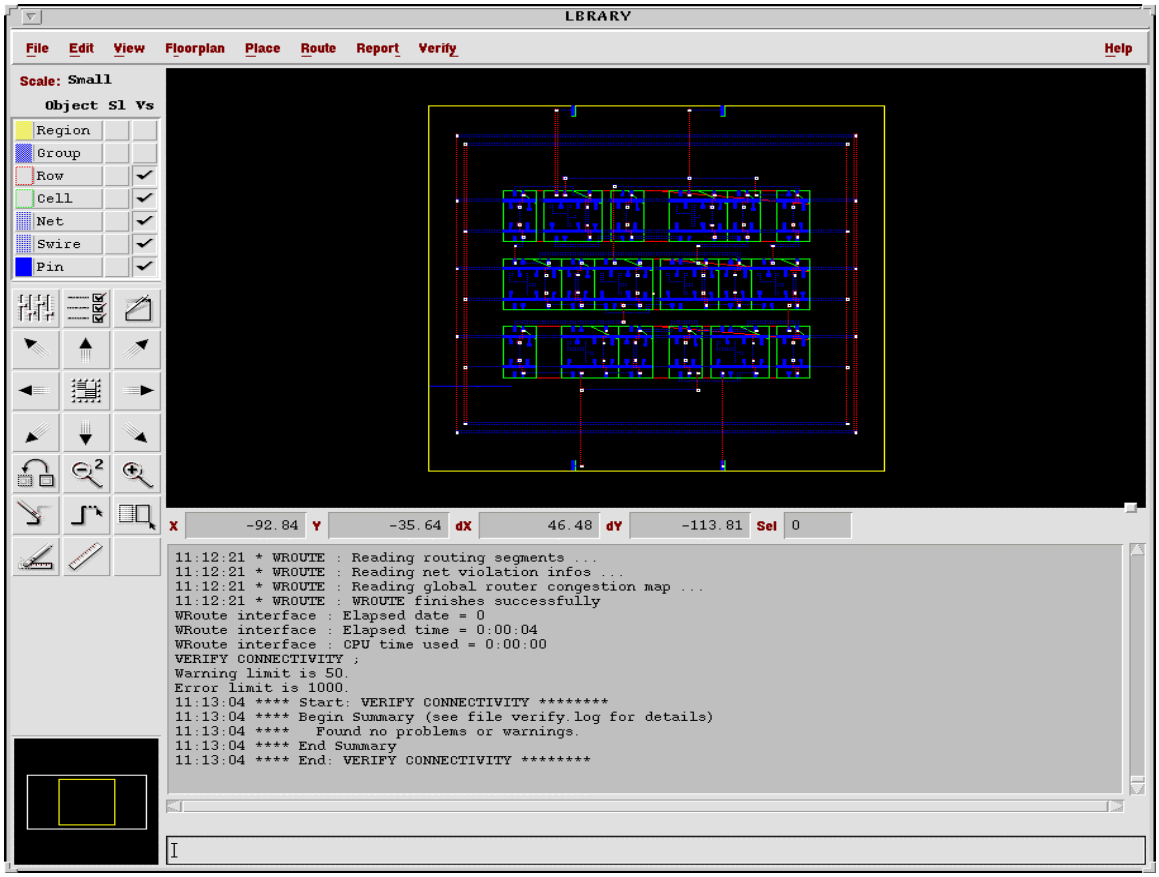

Fig 22: After Verifying Connectivity

b. In Fig 22 select ***Verify –> Geometry.*** The "Verify Geometry" window opens as shown in Fig 23. In Fig 23 click ***OK***. See to it that there are no errors or violations in the command text window. The command text window after verifying geometry is shown in Fig 24.

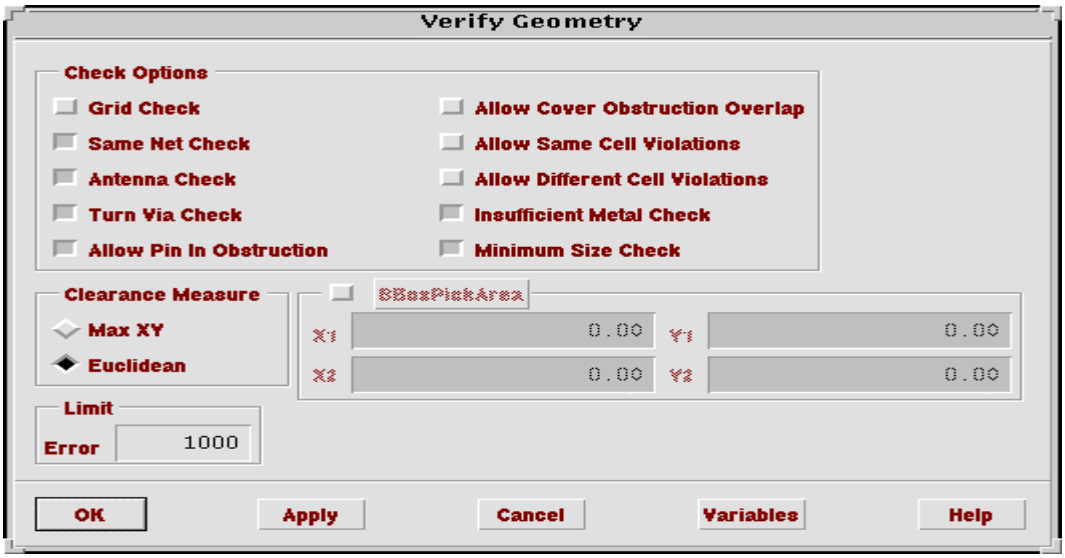

Fig 23: Verify Geometry

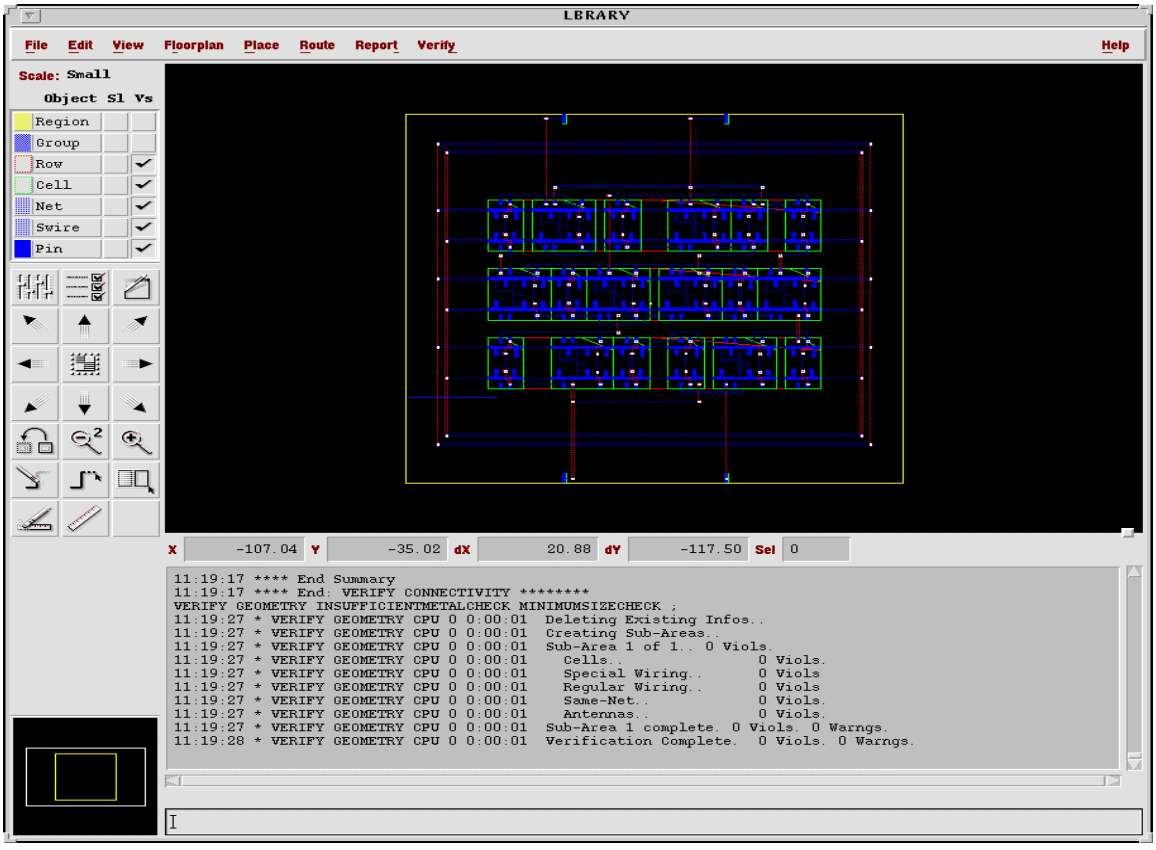

Fig 24: After verifying geometry

Fig 24 also shows the final routed layout.

8. Export File:

This layout has to be exported to cadence.

a. We need to export this layout in GDS-11 format. In Fig 24 select ***File –> Export –> GDS-11***.

b. The "Export GDS-11" window opens as shown in Fig 25. In Fig 25 select **GDS-11 File** and fill an appropriate file name.

c. The gds2.map file should be present in the silicon ensemble directory. Select **Map File** and fill the appropriate path for the gds2.map file.

d. Click ***OK***. Thus the .gds2 file is created.

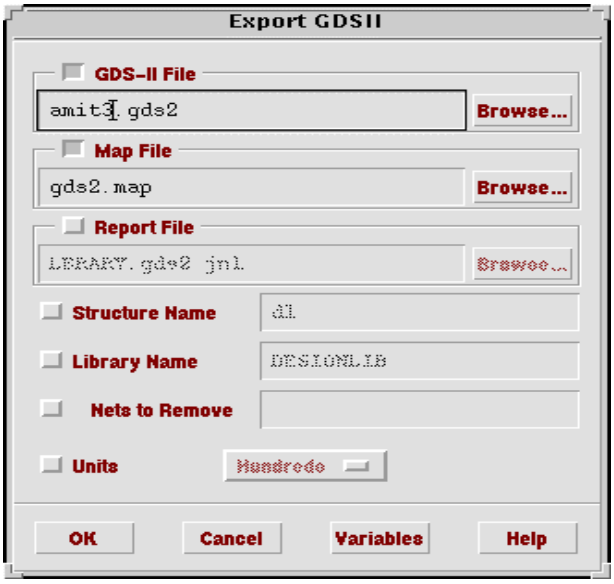

Fig 25: Export GDS11

9. Exit Silicon Ensemble :

In Fig 24 select ***File –> Save*** from the main menu to save the current session and then select ***File –> Exit***.

Importing the GDS-11 file in Cadence:

The .gds2 file created in silicon ensemble has to be imported in cadence.

1. In the icfb window select ***File –> Import –> Stream***.
2. The "Virtuoso Stream In" window opens as shown in Fig 26. In Fig 26 write the path of the .gds2 file created in silicon ensemble in the **Input File** text box.
3. Write the name of the top cell in the **Top Cell Name** text box.
4. Write the library name in the **Library Name** text box.

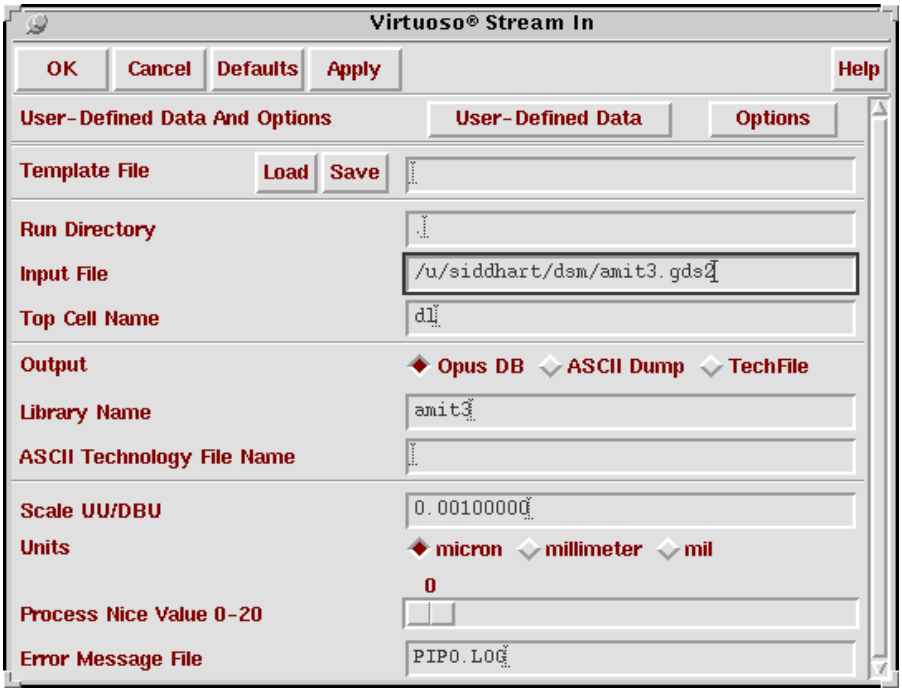

Fig 26: Virtuoso Stream In

5. In Fig 26 click ***Options*** and the "Stream In Options" form opens as shown in Fig 27. In Fig 27 select **Retain Reference Library (No Merge) , Snap XY To Grid Resolution** and click ***OK***.

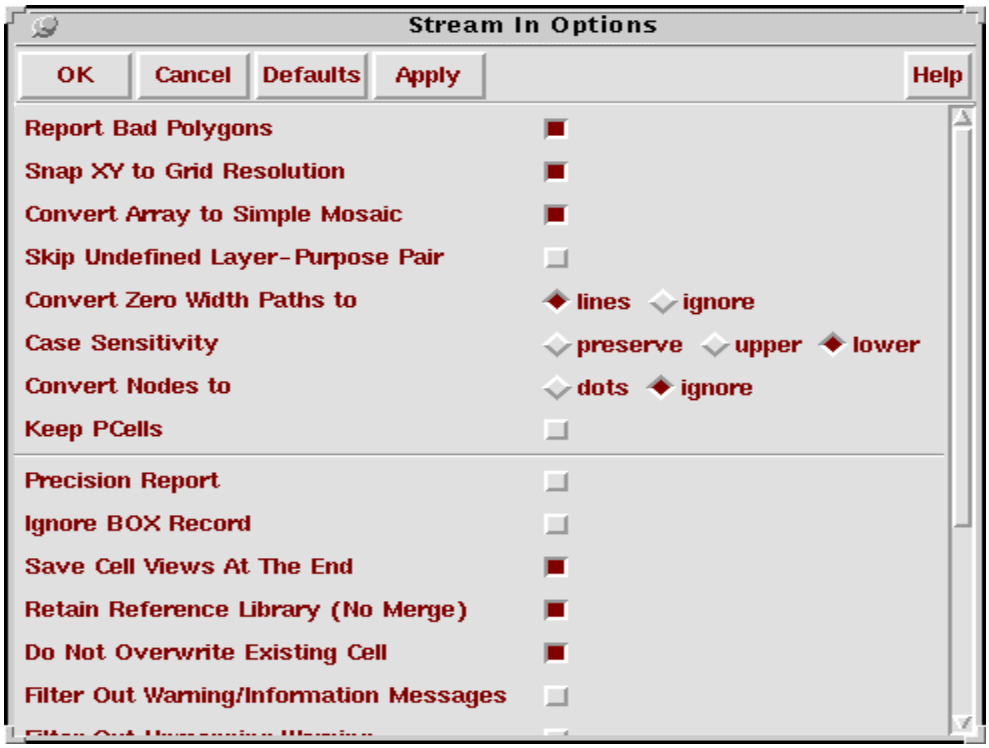

Fig 27: Stream In Options

6. In Fig 26 click ***OK***.

7. Wait for some time as the stream in procedure takes some time. You will get a message that STRMIN completed successfully with 0 errors and 1 warning. This "STRMIN PopUp Message" is shown in Fig 28. If you get more than one warning then there is some problem. Read the icfb window to see the problem.

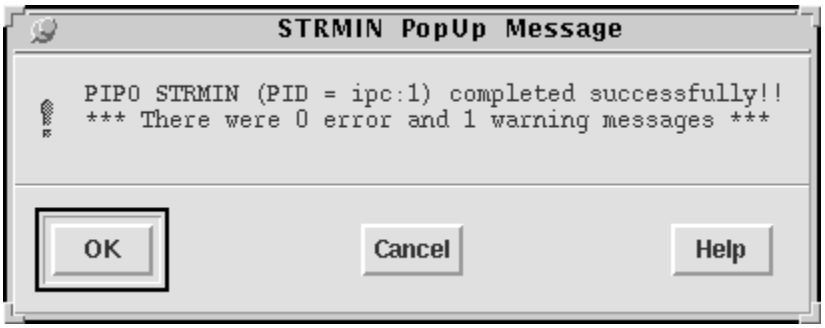

Fig 28: STRMIN PopUp Message

8. If you don't get any errors and you get only one warning then everything is fine. Click ***OK*** in Fig 28.
9. In the library manager open the layout view of the intended design. The layout is as shown in Fig 29.

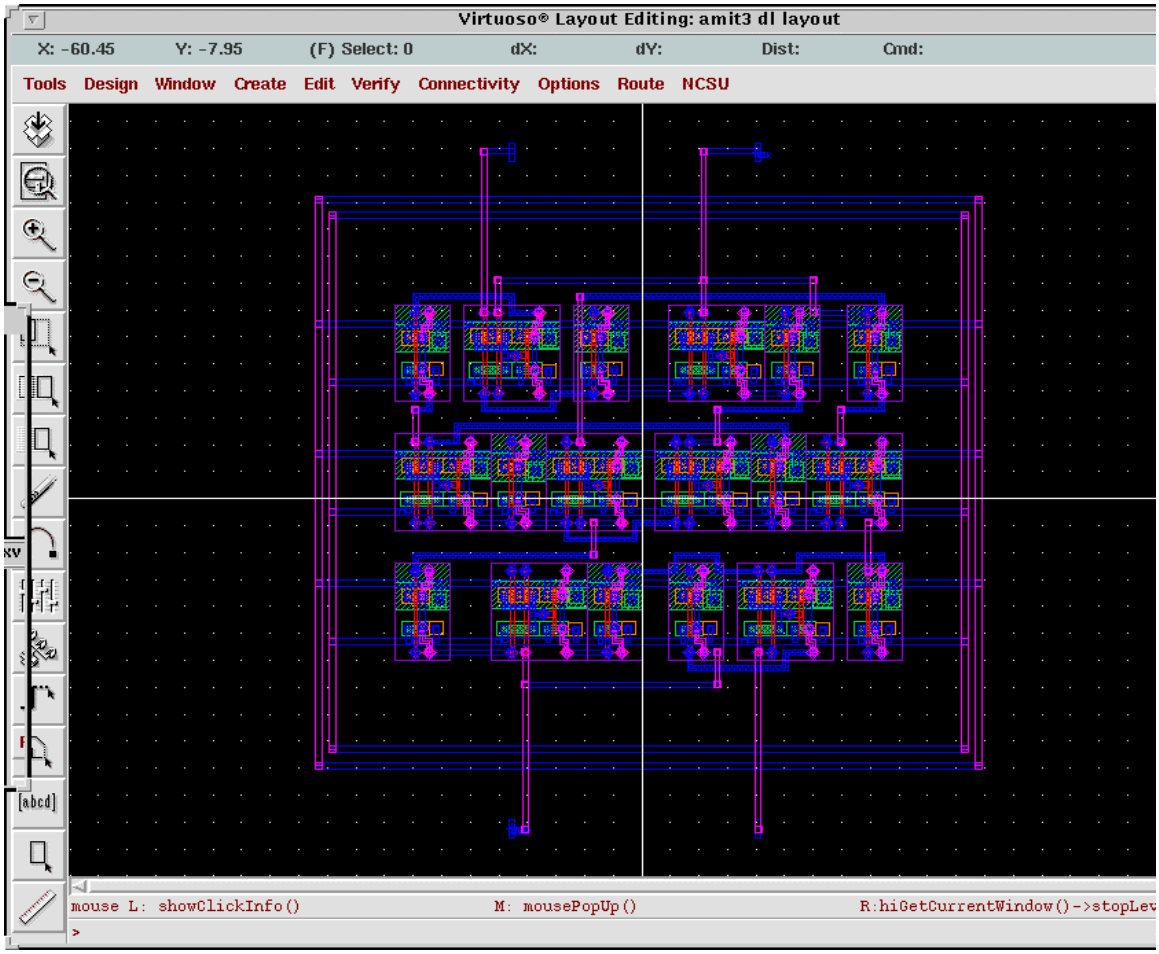

Fig 29: Final Layout

10. In Fig 29 select ***Create –> Pins from Labels*** and the "Create Pins From Lables" window opens as shown in Fig 30. In Fig 30 change the **Pin Layer** for all the **Labels Found** to *metal1 dg* and change the **Width** and **Length** to 0.45. Click ***OK***.

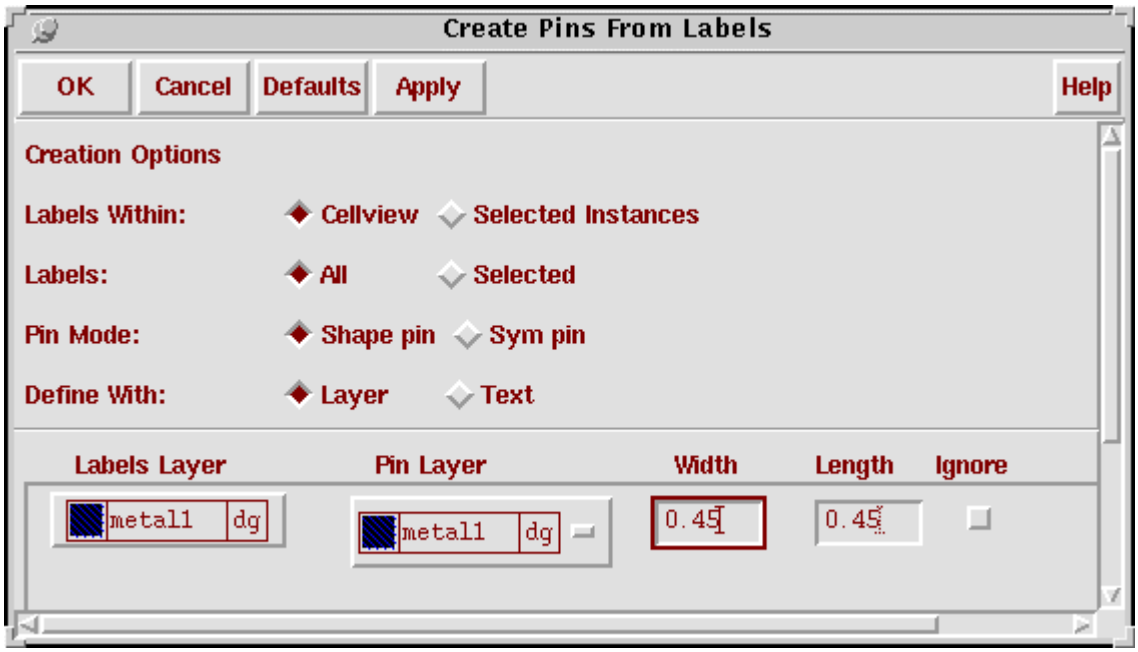

Fig 30: Create Pins From Labels

11. When you export the routed layout from the silicon ensemble to the Virtuoso in the GDS-11 format all the pin labels are in the metal1 dg.
12. Change the layer of the labels from metal1 to *text drawing*.
13. The connectivity of all the pins in the layout is input-output. So change the connectivity of the pins according to the schematic.
14. Add vdd! and gnd! pins manually on the power and ground rings of the generated layout.
15. Now you can perform DRC and LVS on your design.