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Standard Cell based Automatic placing and routing using Verilog netlist in Silicon Ensemble:

Files needed for automatic placement and routing in silicon ensemble:

- 1. LEF file created using Abstract Generator.
- 2. Verilog netlists for all the schematics right from the top hierarchical design to all the standard cells.

1. Start Silicon Ensemble:

Start the silicon ensemble design environment by typing the following:

Hostname.ece.pdx.edu > sedsm - m = 500

Here 500 is the memory allocated for silicon ensemble. The "Silicon Ensemble" window opens as shown in Fig 1.



Fig 1: Silicon Ensemble

2. Import Files:

You will have to import the LEF file which is created using the Abstract generator and also the verilog netlists.

- a. Importing LEF file:
- 1. In Fig 1 select *File -> Import -> LEF*.
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- 2. The "Import LEF" window opens as shown in Fig 2. Select your LEF file.
- 3. Also select Clear Existing Design Data and click OK to import the LEF file.
- 4. Watch the command text at the bottom of the main window to make sure there are no errors in the LEF file. You should see something like this if the .lef file was imported successfully:

##-I No errors found. The database created successfully. Thus importing of the LEF file is done.

Import LEF	
Filter	
*.lef	
Directory and File List	
[Up one directory] .abstract/ .hld/ STD.lef amit1.lef amit2.lef amit3.lef amit3/	
amit4.lef Selection	
/u/siddhart/dsm/amit3.lef	
Report File	
importlef.rpt	Browse
Options	
📕 Clear Existing Design Data 🗐 Expand Pat	hs
🔟 Case Sensitive Names	
OK Apply Cancel Variabl	es Help

Fig 2: Import LEF

- b. Importing Verilog netlist:
- 1. In Fig 1 select *File -> Import -> Verilog*.

Silicon Ensemble using verilog netlists	Tutorial 4 Release Date: 01/13/2005(Version 2)								
		mport Verilog		- .					
	Verilog Sou								
	Ĭ.		Browse						
	Verilog Top								
	Compiled ¥	braries —							
	cds_vbin	Ĭ.							
	Compiled ¥	erilog Output Libra	y						
	cds_vbin								
	Options —								
	Power Nets	vdd!							
	Ground Nets								
	Logic 1 Net	vdd!							

gnd!

Cancel

vdd! gnd!

Logic # Net

Special Nets

ОΚ

Fig 3: Import Verilog

Variables

Help

2. The "Import Verilog" window opens as shown in Fig 3. In the **Verilog Source Files** text box select all the verilog netlists that are needed for your design. Fig 4 shows all the selected netlists.

- 3 -



Fig 4: Selecting the Verilog netlist's

- 3. Click *OK* in Fig 4. In the "Import Verilog"(Fig 3) window enter the name of the primary module in the **Verilog Top Module** text box. This is the name of the hierarchial top module in the verilog netlist.
- 4. In the **Compiled Verilog Reference Libraries** text box just type *cds_vbin*.
- 5. Replace vdd! and gnd! with vdd and gnd for all the categories in "Import Verilog" form as shown below.

Silicon Ensemble using verilog netlists	Re	Tutorial 4 lease Date: 01/1	13/2005(Ve	rsion 2)
г -	Í II	mport Verilog		
	Verilog Sou	r ce Files /tsmcl/3. vį́	Browse	
	ckt1	i module		
	Compiled H	esiles Deference Lil		
	čompneu v	ernog kelerence Lu	oraries	
	Compiled V	erilog Output Librar	У <u> </u>	
	cds_vbin			
	Options			
	Power Nets	vdď		
	Ground Nets	gnđ		
	Logic 1 Net	vdď		
	Logic I Net	gnđ		
	Special Nets	vdd gnđ		
	ок (Cancel Variables	Help	

Fig 5: Completed Import Verilog form

6. After completing all these steps the form shown in Fig 3 looks as shown in Fig 5. Click *OK*. Watch the command text box to make sure there are no errors in importing the verilog netlist. Thus importing of the verilog netlists is done.

3. Floorplanning:

a. In "Silicon Ensemble" window select *Floorplan –> Initialize Floorplan* to open the floorplanning window. The window appears as shown in Fig 6.

Silicon Ensemble using	Tutorial 4
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r ⁷		Init	ialize Floorplan		
Design Statistic Number of: Cells IO Pads Corner Pads Area (Square Cells	18 Blocks O IO Pins ds O Nets e Microns) 4147.20	0 4 22	Die Size Constraint Aspect Ratio Height Width Fixed Size	AspectRatio	1.0
- IO To Core Dist	microns	0.00	Core Area Parameters	tracks	85.0
Top/Bottom	microns 🖃	0.00	Block Halo Per Side	microns _	20.00
Calculate Exp	ected Results				
ок	Apply]	Cancel	Variables	Help

Fig 6: Initialize Floorplan

- b. In **Die Size Constraint** field the **AspectRatio** is set to 1. You can change the aspect ratio to change the ratio between height and width of the design.
- c. Set the **IO To Core Distance** to 20 microns for both directions. If the design has room after routing you can change this distance and rerun the whole procedure after floorplanning again.
- d. In the **Core Area Parameters** the **Row Spacing** controls the distance between two rows. You can initially set this distance as 5 microns. You may reduce this afterwards to shrink the design area.
- e. Set the **Block Halo Per Side** to 2 microns.
- f. Row Utilization is set to 85% as default value.
- g. Click the *Calculate* button to view the preliminary floorplan summary in the Expected Results text window. The "Initialize Floorplan" window now appears as shown in Fig 7.

- 6 -

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	Init	ialize Floorplan		,
Design Statistics Number of: Cells 18 Blocks IO Pads 0 IO Pins Corner Pads 0 Nets Area (Square Microns) Cells 4147.20	0 4 22	Die Size Constraint Aspect Ratio Height Width Fixed Size	AspectRatio	1.0
I off / Pinht minner of	cin nn	Core Area Parameters		85.0
	2:0.00	Row Spacing Block Halo Per Side	microns 💷	5 <u>,</u> 00 2 <u>,</u> 00
	40.00	- Flip Every Other Row		Abut Rows
Aspect Ratio: 1.00 Width: Core row utilization = 100. Chip Area = 13572.25 sq. mi IO to Core Distance (micron Number of Standard Cell Row Design is core-limited.	116.50 micro 39≋. .crons. us): X: 20.0 vs = 3.	ns, Height: 116.50 mi	crons.	
ОК Арріу		Cancel	Variables	Help

Fig 7: Initialize Floorplan

- h. In Fig 7 reduce the **Row Utilization** parameter and re-calculate until the reported Core row utilization is less than 100%.
- i. After the **Row Utilization** is reduced and the floorplan is recalculated the initialize floorplan window appears as shown in Fig 8.
- j. In Fig 8 click **OK** to finalize the floorplan.

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۲ ^۲ Initi	ialize Floorplan		-
Design Statistics Number of: A Cells 18 Blocks O IO Pads O IO Pins 4 Corner Pads Nets 22 Area<(Square Microns) Cells 4147.20	Die Size Constraint Aspect Ratio Height Width Fixed Size	AspectRatio	1.0
IO To Core Distance Left / Right microns 20.00 Top/Bottom microns 20.00	Core Area Parameters Row Utilization(%) Row Spacing Block Halo Per Side	microns 🖃	65 <u>.</u> 0 5 <u>.</u> 00 2 <u>.</u> 00
Calculate Expected Results Aspect Ratio: 1.00 Width: 127.83 micror Core row utilization = 65.58%. Chip Area = 16340.51 sq. microns. IO to Core Distance (microns): X: 20.00 Number of Standard Cell Rows = 4. Design is core-limited.	ns, Height: 127.83 micr D Y: 20.00	ons.	
OK Apply	Cancel	/ariables	Help

Fig 8: Final Floorplan

k. You will see the rows placed as shown in Fig 9. Thus the floorplanning is done.

Silic	on E erilo	lnsen g net	nble us tlists	sing			Re	T lea	utorial 4 se Date:	4 01	./1	3/2005(V	ersi	on 2)	-
									L	BRA	RY				
File	Edit	View	Floorplan	Place	Route	Report	Verif	Y.							
Scale: Of	Small	l Sl Vs													
Gro Rov	yion Dup 7														
Cel Net	Ll C	~ ~													
Pir H.H.	1 	- 1													
	G														
-	譿	-													
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£	ଙ୍	¢													
N N	יר //														
	<u></u>		x	-58.7	8 Y	-3.	7.24	dX	42.	73	dY	-103.24	Sel	0	

Fig 9: Rows after Floorplanning

4. Placement:

Once the floorplanning is complete, IO ports and cells need to be placed in the allotted rows.

a. In Fig 9 select *Place -> IOs*. The "Place IO" window opens as shown in Fig 10. In Fig 10 make sure that the **Placement Mode** is set to **Random** and **Space**: **Evenly** is selected. Click *OK*. The IOs will be placed.

	Place IO
Placement Mode	
* Random	
🔷 I/O Constraint File	oplace.iot Write Est
\diamond Refine Pin Placemer	nt i kana pina on azme zide
— 🖵 Pin Layer Assignm Top / Boltom	metail 💷
Leff / Right	metal -
Space : 🗢 Evenly <	Abutted 🔷 Center Abutted
OK	Cancel Help

Fig 10: Place IO

- 10 -

The placement of the IOs is as shown in Fig 11.

									LBRA	٩RY						
File	Edit	View	Floorplan	Place	Route	Report	Verify									
Scale	: Smal	1										Î.				
0	bject	Sl Vs														
Re	gion															
Gr	oup															
Ro	w 	_ ✓														
Ne	t	-														
Sw	ire	~														
Pi	n	✓														
្ធម្នា		1														
1742																
	1911															
	3.#3															
×	₩															
£	୍	÷.														
\mathbf{N}	പ															
		′ `														
			x	-40.4	6 Y	-38	. 84 d)	¢ 📃	61.05	dY	-104.84	Sel	0			
			12:59:5	52 Begi	n IOPL	ACE										
			REFRESH 12:59:5	i 52 IOPL	ACE fi	nished.										
			-								 			 	 	
			1													

Fig 11: IOs Placed

b. In Fig 11 select *Place -> Cells* and the "Place Cells" window opens as shown in Fig 12. In Fig 12 click *OK*. The cells will be placed as shown in Fig 13. If there is an error saying that Impossible to Place without Overlaps, go back to floorplanning and reduce the row utilization and repeat the procedure from floorplanning.

Place Cells										
🔲 Timing Driven Plac	ement									
🔲 Power Driven Plac	ement									
🗐 Timing Analysis	Report File									
🗐 Pin Placement										
🔲 Generate Congesti	on Map									
Optimize :										
🗖 Timing 🔲 Signal	l Integrity 🔄 Scan Chains									
Options	Report File LERARY, quopt, spt									
OK Cance	I Options Variables Help									

Fig 12: Place Cells Portland State University

Silicon Enser verilog ne	nble usir tlists	ıg		Tutorial 4 Release Date: 01/13/2005(Version 2)	-
				LBRARY	
<u>File Edit View</u>	Floorplan P	lace <u>R</u> oute	Report	Verify	
Scale: Small Object SI VS Region Oroup Row Cell Net V Swire Pin Pin A A A A A A A A A A A A A					
	Y Place int Place int Place int	53.20 Y erface : H erface : H erface : C	-1 lapsed lapsed PU time	8.40 dX 48.31 dY -84.40 Sel 0 date = 0 time = 0:00:04 used = 0:00:00	

Fig 13: Cells after placing

5. Power/Ground Routing:

a. In Fig 13 select *Route -> Plan Power* and the "Plan Power" window opens as shown in Fig 14. In Fig 14 click *Add Rings*.



Fig 14: Plan Power

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b. The "Add Rings" window opens as shown in Fig 15. In Fig 15 set the **Core Ring Width** to 1.2 microns and click *OK* to apply the rings and close the "Plan Power" window. The **Core Ring width** can be set to be a multiple of 1.2. Fig 16 shows that the rings are placed.

1 5	vuu				
Ring	Layer	Core Ring Width	Core Ring	Spacing	Block Ring Widt
Horizontal	metal 1 💷	2.700	Center 💴	0.000	0.000
Vertical	metal2 💷 🗍	2.700	Center 💷	0.000	0.000
Nets					
Netz Ring	Layor	Care Ring Width	Core Ring	Spacing	Black Ring Width
Netz Ring Harizontzi	Layer metal1 💷	Core Ring Width	Core Ring Center 🔟	Spacing	Slock Ring Width

Fig 15: PP Add Rings



Fig 16: Cells with Rings

c. In Fig 16 select *Route -> Connect Ring* and the "Connect Ring" window opens as shown in Fig 17. In Fig 17 click *OK*. This will connect your power and ground rings to your cell rows. Fig 18 shows that the cell rows are connected to the power and ground rings. Thus the Power and Ground routing is done.

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Conn	ect Ring	
Nets "gnd" "vdd"		
🗖 Stripe		
🗖 Block 🗖 All Ports	💷 Maximum Width	0.000
	Selected Blocks	
🗖 IO Pad 🛛 🗖 All Ports	🔲 Maximum Width	0.000
🗖 IO Ring	💷 Pin Width	0.000
Follow Pins	💷 Pin Width	0.000
OK Apply C:	ancel Variables	Help

Fig 17: Connect Ring



Fig 18: Rings after being connected

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a. In Fig 18 select *Route -> WRoute*. The "WRoute" window opens as shown in Fig 19. Make sure that Global and Final Route and Auto Search And Repair are selected and click *OK*. This will do the routing of the cells. Fig 20 shows the cells after routing.

	WRoute
Routing Mode	
🔷 Global Route Only	
🔶 Global and Final Route	🗖 Auto Search And Repair
🔷 Incremental Final Route	🛛 🗆 Redo Global Naule for visiationo
I Timing Driven Routing	
OK Cancel	Options Variables Help

Fig 19: WRoute



Fig 20: Cells after Routing

7. Verify:

a. In Fig 20 select *Verify -> Connectivity*. The "Verify Connectivity" window opens as shown in Fig 21. In Fig 21 click *OK*. See to it that there are no errors or warnings in the command text window. The command text window after verifying connectivity is shown in Fig 22.

Verify Connectivity					
🔲 Search For All L	Jnverifi	ied Connectivity			
Туре		BBozPickársz			
🗢 All	×1	0.0	0 _{¥1}		0.00
🔷 Regular Only	×2	0.0	0 42		0.00
◇ Special Only					
Nets					
🔶 All					
🔷 By Name					
Limite					
Error					1000
Warning					50
ОК	Арр	ly Cancel		Variables	Help

Fig 21: Verify Connectivity



Fig 22: After Verifying Connectivity

b. In Fig 22 select *Verify -> Geometry*. The "Verify Geometry" window opens as shown in Fig 23. In Fig 23 click *OK*. See to it that there are no errors or violations in the command text window. The command text window after verifying geometry is shown in Fig 24.

	Verify Geometry	
Check Options		
🔟 Grid Check	Allow Cover Obstruction Overlap	
🔲 Same Net Check	Allow Same Cell Violations	
🔲 Antenna Check	Allow Different Cell Violations	
🔲 Turn Via Check	🔲 Insufficient Metal Check	
🔲 Allow Pin In Obstruct	on 🗖 Minimum Size Check	
Clearance Measure —	BBoxPickArea	
🔷 Max XY	X1 0.00 ¥1	0.00
🔶 Euclidean	X2 0.00 Y2	0.00
Limit		
Error 1000		
OK A	piy Cancel Variables	Help

Fig 23: Verify Geometry



Fig 24: After verifying geometry

Fig 24 also shows the final routed layout.

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8. Export File:

This layout has to be exported to cadence.

- a. We need to export this layout in GDS-11 format. In Fig 24 select *File -> Export -> GDS-11*.
- b. The "Export GDS-11" window opens as shown in Fig 25. In Fig 25 select **GDS-11 File** and fill an appropriate file name.
- c. The gds2.map file should be present in the silicon ensemble directory. Select **Map File** and fill the appropriate path for the gds2.map file.
- d. Click **OK**. Thus the .gds2 file is created.

, E	xport GDSII	
🗖 🗖 GDS-II File —		
amit3[.gds2		Browse
🗖 🗖 Map File ———		
gds2.map		Browse
Report File		
LERARY.gds2 jnl		Brawoe
Structure Name	al.	
🗐 Library Name	DESIGNLIB	
🗐 Nets to Remove		
🗆 Units	Hundrodo 🗖	
OK Can	vel Variables	Help

Fig 25: Export GDS11

9. Exit Silicon Ensemble :

In Fig 24 select *File -> Save* from the main menu to save the current session and then select *File -> Exit*.

Importing the GDS-11 file in Cadence:

The .gds2 file created in silicon ensemble has to be imported in cadence.

- 1. In the icfb window select *File -> Import -> Stream*.
- 2. The "Virtuoso Stream In" window opens as shown in Fig 26. In Fig 26 write the path of the .gds2 file created in silicon ensemble in the **Input File** text box.
- 3. Write the name of the top cell in the **Top Cell Name** text box.
- 4. Write the library name in the Library Name text box.

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🤇 😡 🛛 Vi	rtuoso® Stream In		
OK Cancel Defaults Apply	Help		
User-Defined Data And Options	User-Defined Data Options		
Template File Load Save	V		
Run Directory	, i		
Input File	/u/siddhart/dsm/amit3.gds2		
Top Cell Name	dlī		
Output	◆ Opus DB ◇ ASCII Dump ◇ TechFile		
Library Name	amitä		
ASCII Technology File Name	¥.		
Scale UU/DBU	0.00100000		
Units	🔶 micron 🗇 millimeter 🔷 mil		
Process Nice Value 0-20			
Error Message File	PIPO.LOČ		

Fig 26: Virtuoso Stream In

 In Fig 26 click *Options* and the "Stream In Options" form opens as shown in Fig 27. In Fig 27 select **Retain Reference Library (No Merge)**, **Snap XY To Grid Resolution** and click *OK*.

<u>[</u> @			Strea	m In Options	1	
ок	Cancel	Defaults	Apply	Help	9	
Report B	ad Polygo	ns		—	Ā	
Snap XY	to Grid Re	esolution		F		
Convert /	Array to S	imple Mosa	aic			
Skip Und	efined Lay	er-Purpos	e Pair			
Convert 2	Zero Width	Paths to		🔶 lines 🐟 ignore		
Case Sen	sitivity			⇔preserve ⇒upper ◆lower		
Convert I	Nodes to			🔷 dots 🔶 ignore		
Кеер РСа	ells					
Precision	Report					
Ignore BO	OX Record	l i i			4	
Save Cel	l Views At	The End		—		
Retain Reference Library (No Merge)						
Do Not O	verwrite	Existing Ce		F		
Filter Out Warning/Information Messages				es 🔟		
					¥.	

Fig 27: Stream In Options

- 6. In Fig 26 click **OK**.
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7. Wait for some time as the stream in procedure takes some time. You will get a message that STRMIN completed successfully with 0 errors and 1 warning. This "STRMIN PopUp Message" is shown in Fig 28. If you get more than one warning then there is some problem. Read the icfb window to see the problem.



Fig 28: STRMIN PopUp Message

- 8. If you don't get any errors and you get only one warning then everything is fine. Click *OK* in Fig 28.
- 9. In the library manager open the layout view of the intended design. The layout is as shown in Fig 29.



Fig 29: Final Layout

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10. In Fig 29 select *Create -> Pins from Labels* and the "Create Pins From Lables" window opens as shown in Fig 30. In Fig 30 change the **Pin Layer** for all the **Labels Found** to *metall dg* and change the **Width** and **Length** to 0.45. Click *OK*.

(B	Create Pins F	From Labels		
OK Cancel [Defaults Apply			Help
Creation Options				
Labels Within:	$igstar{}$ Cellview $\langle \rangle$ Selected Ins	tances		
Labels:	🔶 All 🛛 🔷 Selected			
Pin Mode:	🔶 Shape pin 💠 Sym pin			
Define With:	🔶 Layer 🛛 🔷 Text			
Labels Layer	Pin Layer	Width	Length Ignore	•
metal1 dg	metall dg 🖃	0.45	0.45	
				¥
<u>a</u>				Þ

Fig 30: Create Pins From Labels

- 11. When you export the routed layout from the silicon ensemble to the Virtuoso in the GDS-11 format all the pin labels are in the metall dg.
- 12. Change the layer of the labels from metal1 to *text drawing*.
- 13. The connectivity of all the pins in the layout is input-output. So change the connectivity of the pins according to the schematic.
- 14. Add vdd! and gnd! pins manually on the power and ground rings of the generated layout.
- 15. Now you can perform DRC and LVS on your design.

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