Creating a verilog netlist for a schematic:

The verilog netlist is necessary for automatic layout (placement and routing) tools. It contains information about the I/O pins and the connectivity of the entire schematic. Here we have taken an example of two cascaded inverters and the netlists are created for this example. The name of this schematic is inverter.

Important Point:

The names of the schematic and the pins in the schematic should not start with a number and should not be keywords in verilog (e.g. and, nand). The length of the names should not be more than 15 characters. You should not use '+' and '-'signs for the names of the pins and the schematics.

1. Open the Schematic cell view:

From the Library manager read the inverter schematic cell view. Save the schematic. The inverter schematic is shown in Fig 1.

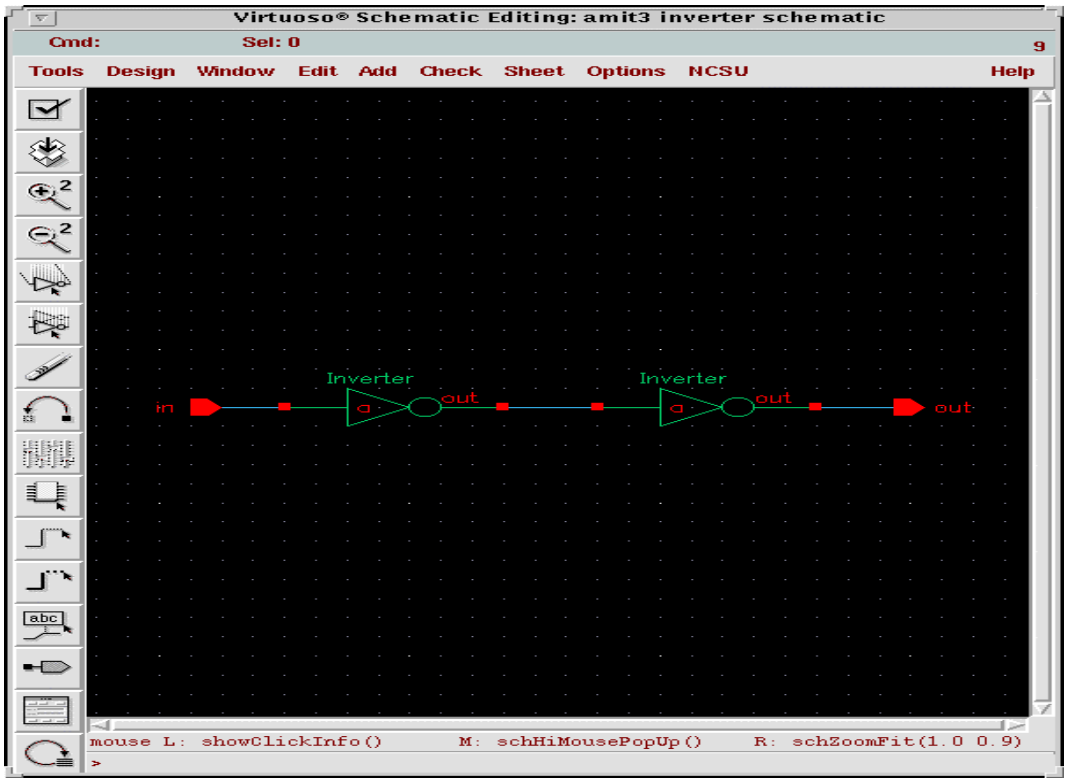


Fig 1: Inverter

2. Initializing Verilog Integration:

a. In Fig 1 select ***Tools –> Simulation –> Verilog - XL*** . The "Setup Environment" window opens as shown in Fig 2.

b. In Fig 2, enter inverter.run1 in the **Run Directory** text box. All other default values are correct. Click ***OK***.

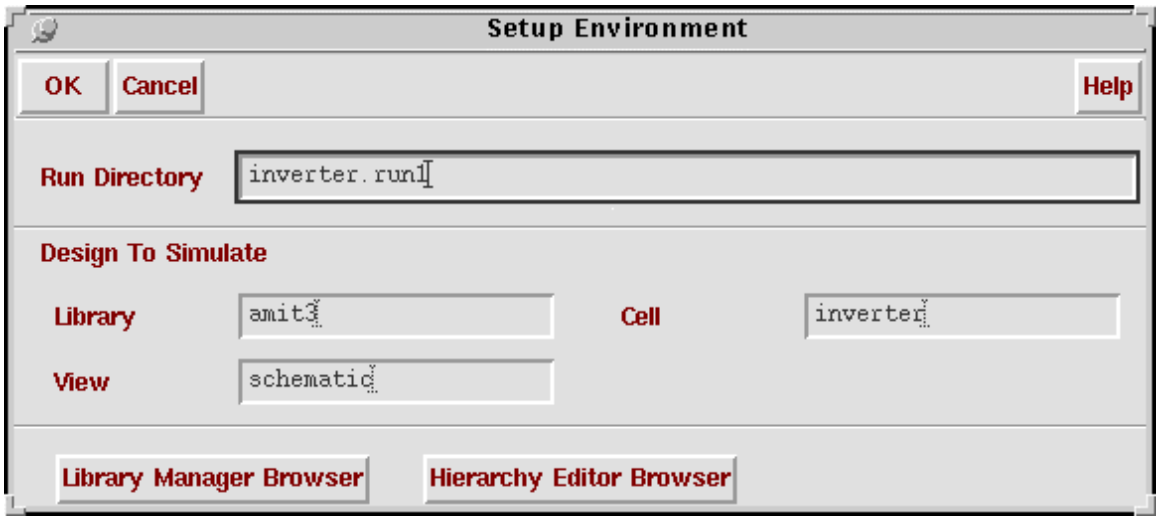


Fig 2: Setup Environment

c. The "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window opens as shown in Fig 4 and the inverter.run1 directory is created.

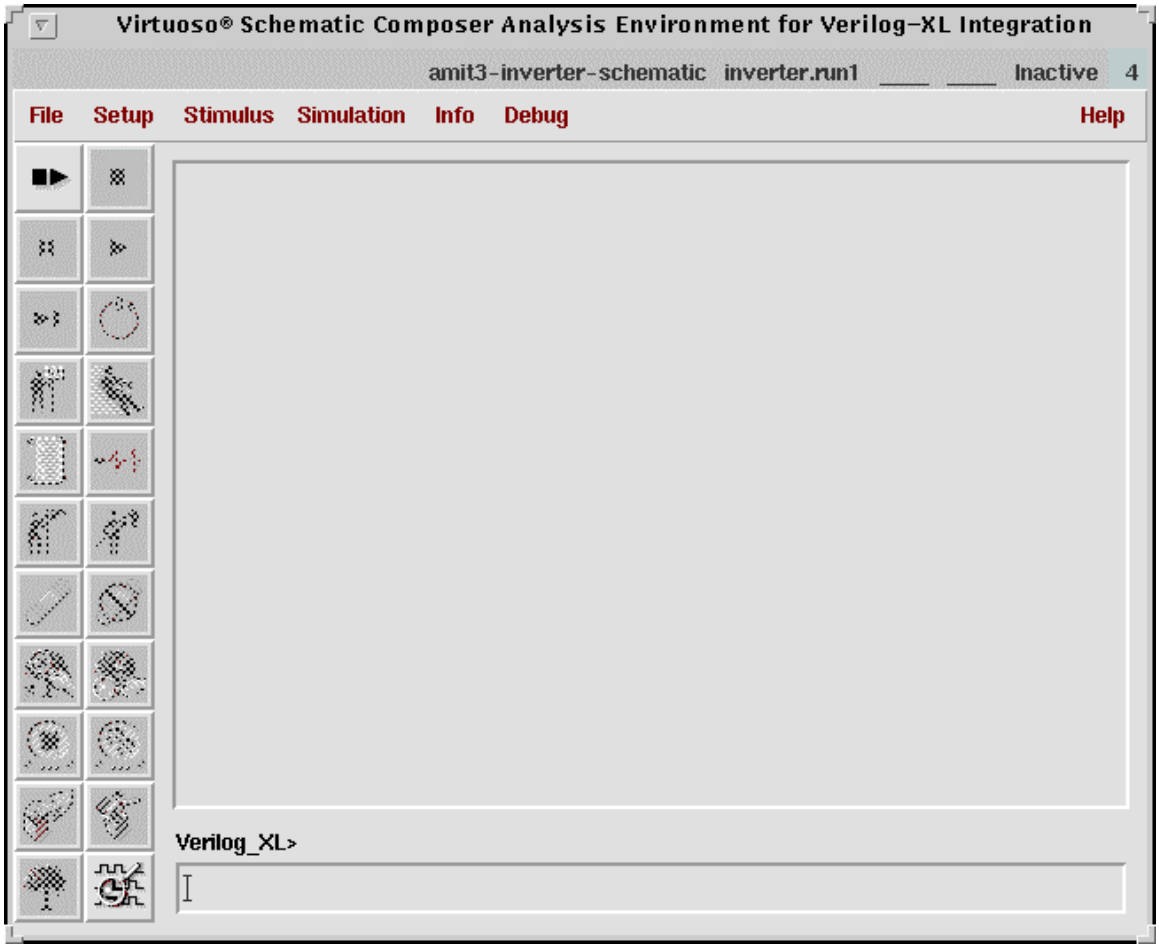


Fig 4: Environment for Verilog-XL Integration

3. Setting the Netlist Options:

a. In Fig 4 set the netlisting options by selecting ***Setup –> Netlist***. The "Verilog Netlisting Options" form opens as shown in Fig 5.
b. The default settings are as shown in Fig 5. They are all correct.

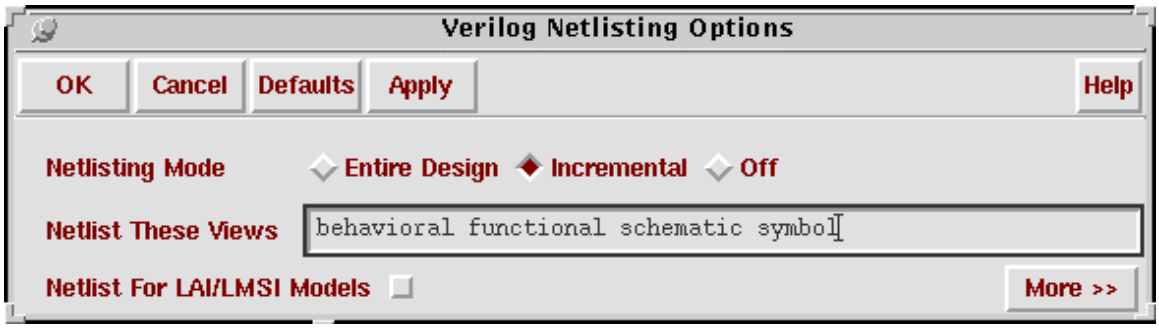


Fig 5: Verilog Netlisting Options

c. In Fig 5 click ***More>>***
Additional netlisting options are added to the form as shown in Fig 6.

d. In Fig 6 set **Global Power Nets** to *vdd* and set **Global Ground Nets** to *gnd*..
e. Select **Generate Pin Map**.
f. The **Drop Port Range** and **Preserve Buses** options are selected by default. It doesn't matter if we select or deselect them.
g. Click ***OK***. Thus setting the Verilog Netlisting Options is done.

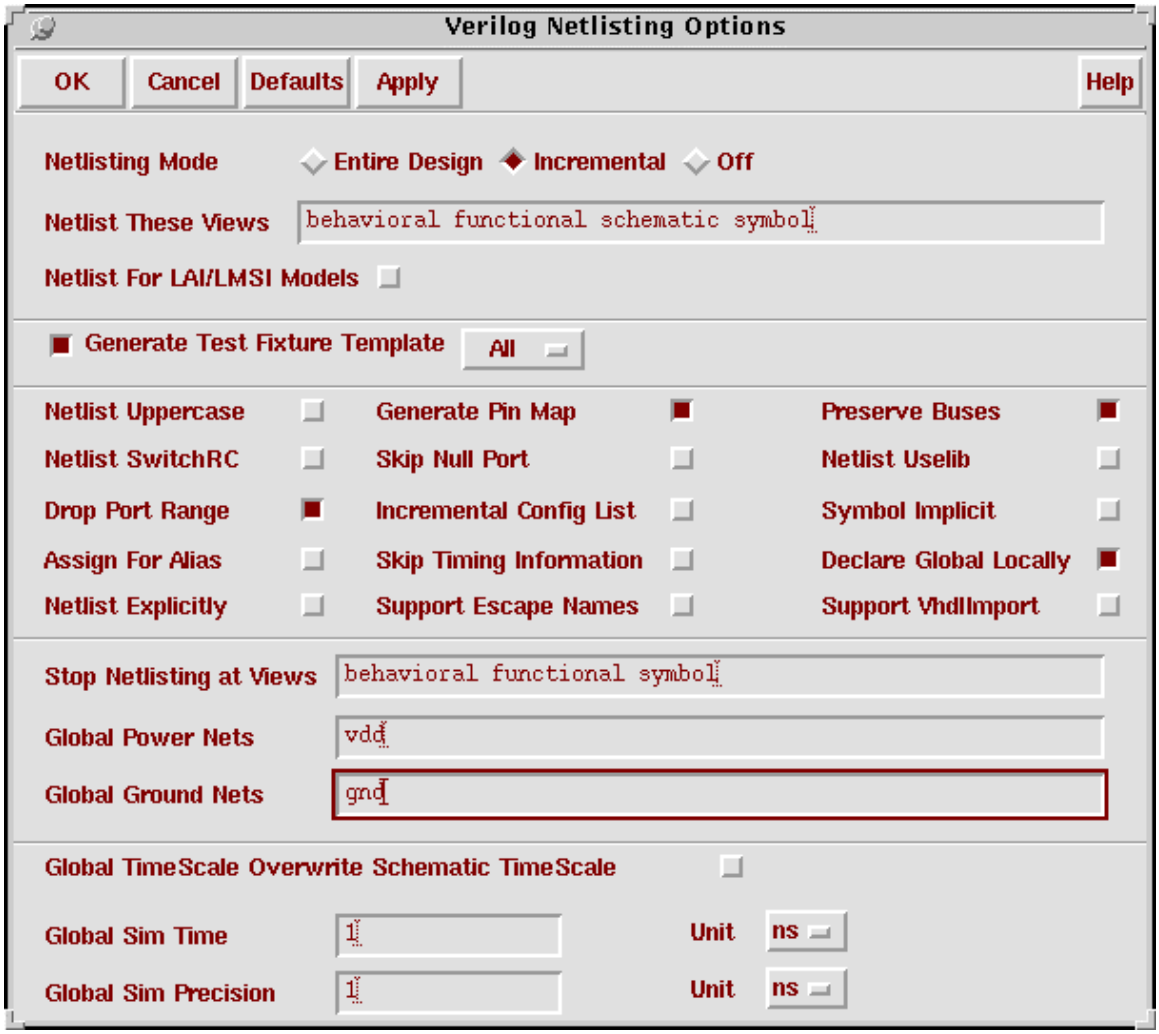


Fig 6: Additional Verilog Netlisting Options

4. Creating the Stimulus File:

a. In the "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window select ***Stimulus –> Verilog.***
b. A dialog box appears as shown in Fig 7. Click ***Yes*** in the dialog box.

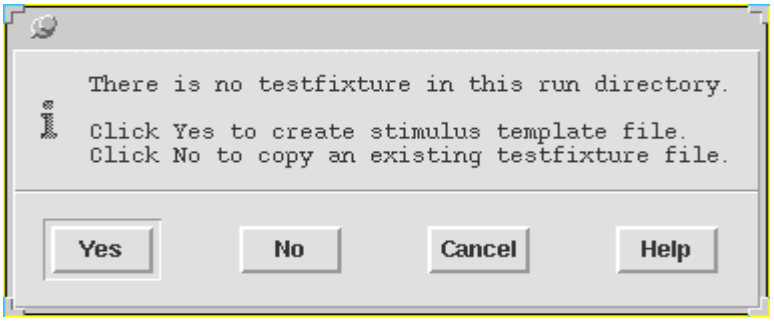


Fig 7: Dialog Box

c. A "Stimulus Options" form opens as shown in Fig 8. Select **textfixture.verilog** as the **File Name** and then click ***OK***.

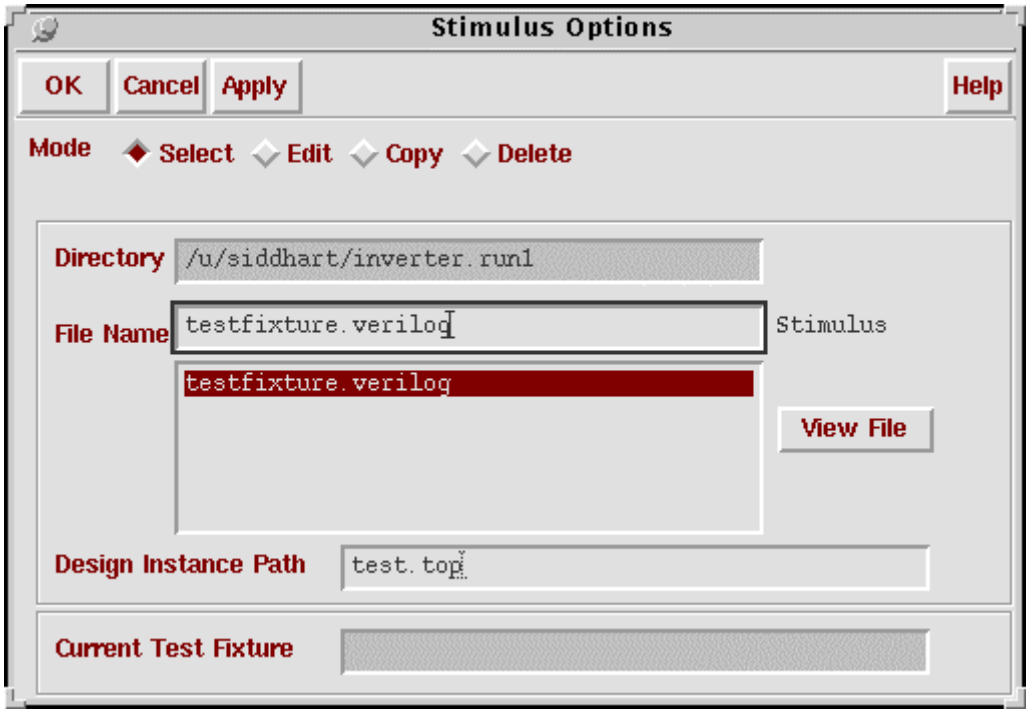


Fig 8: Simulation Options

d. Thus the netlist is created for the schematic.

5. Creating the Verilog Files :

Now we need to make the verilog files from the netlists which are created.

a. In the "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window select ***File -> View Netlist Result -> Netlist Run Files ….*** The "View Netlist Run Files" window appears as shown in Fig 9.

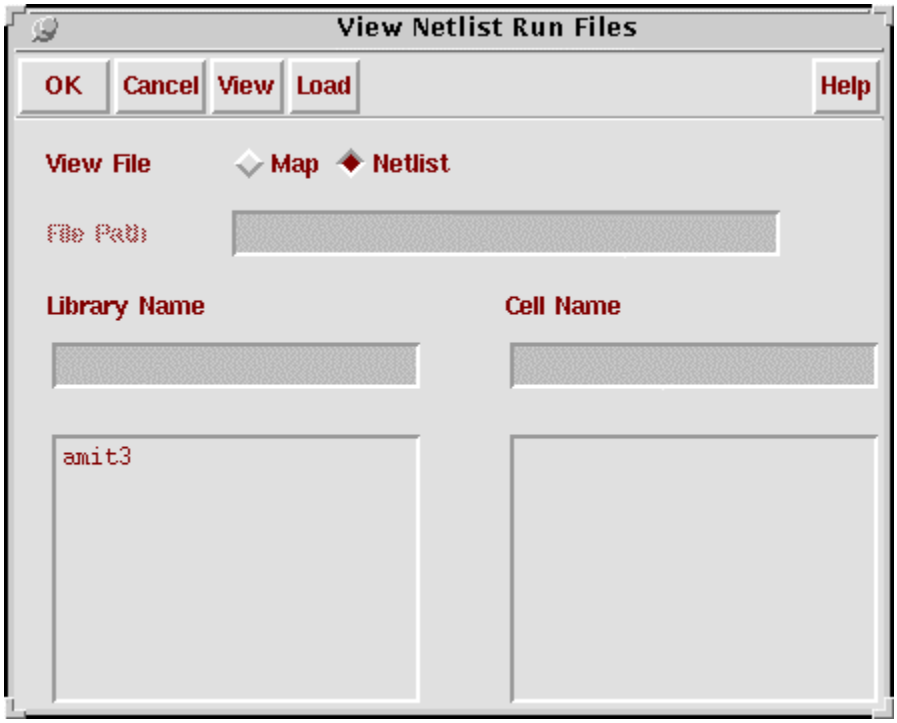


Fig 9: View Netlist Run Files

b. In Fig 9 click on the **Library Name** appearing in the left box (e.g. amit3). The cells in that directory should appear in the **Cell Name** box as shown in Fig 10.

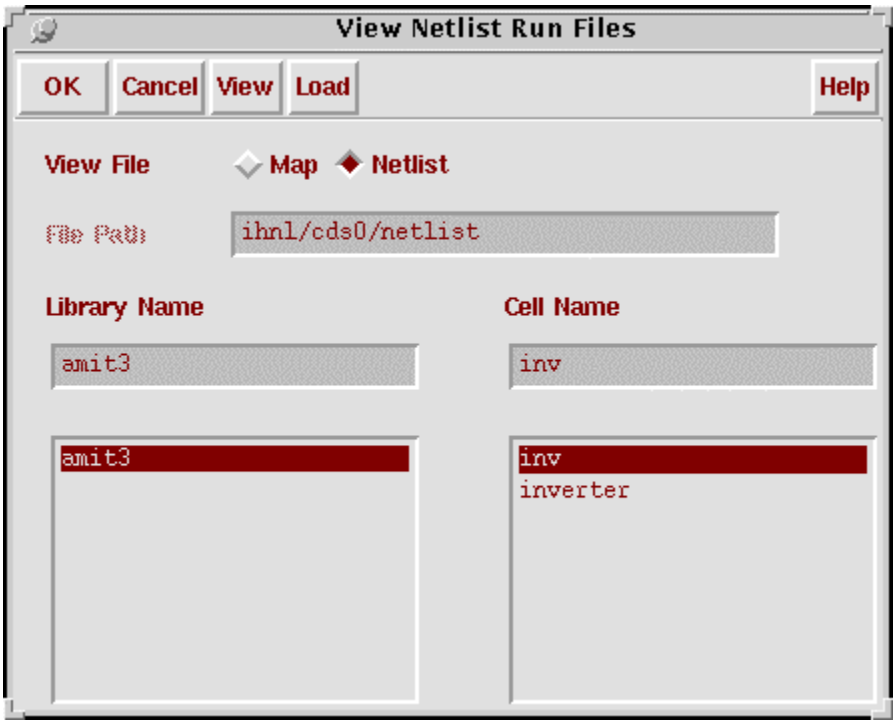
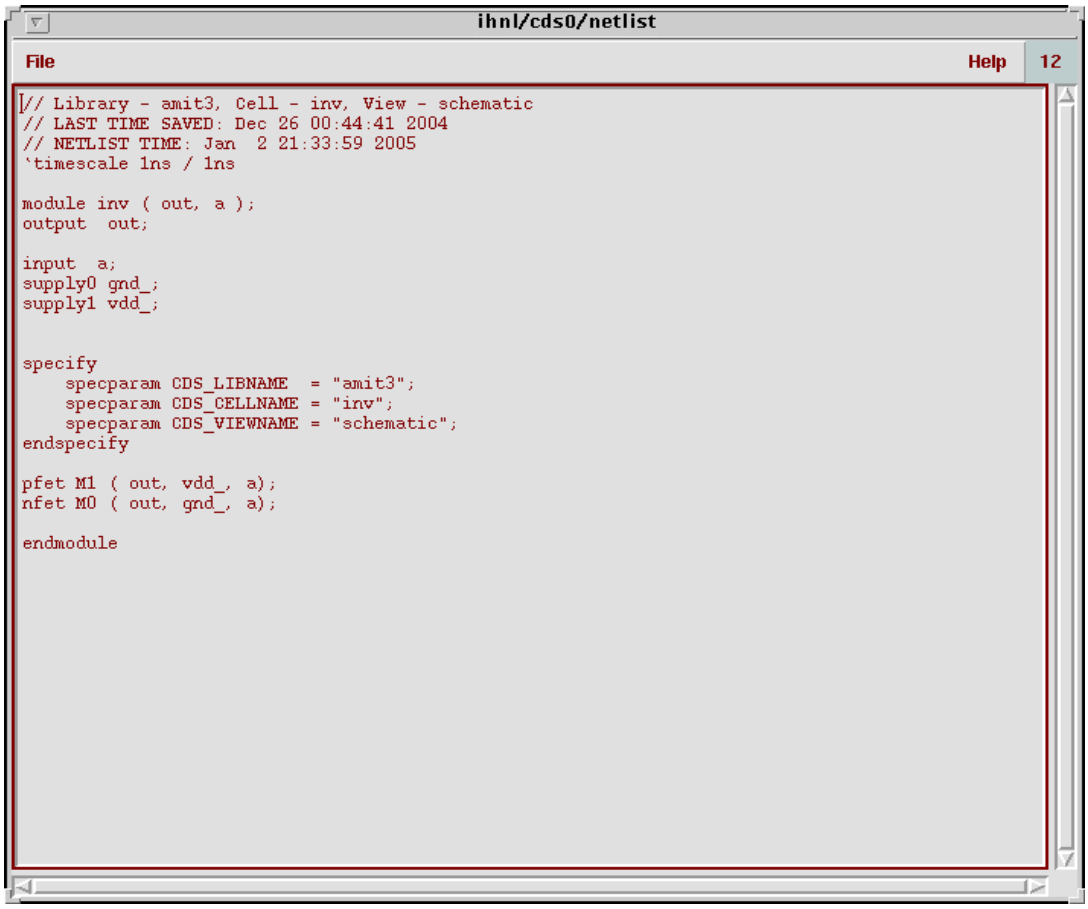


Fig 10: Viewing Cells

c. In Fig 10 click on the cell name (e.g.: inv) and then click **View**. The netlist opens as shown in Fig 11.



d. Now save these netlist as a verilog file by selecting ***File -> Save As…***. Save the file with a .v extension and at a location of your wish.
e. Save the netlists of all the cells in a similar way.

Thus the verilog netlists for your design have been created. Now use Tutorial 4 to do placement and routing using Silicon Ensemble.