# Abstract Generation:

### **Export GDS:**

Abstract generator comes as a part of the Silicon Ensemble package. As such, it cannot directly read ICFB library databases. We need to export the standard cell library to Stream (GDS) format and then re-import the GDS file in Abstract Generator. To export to GDS format from ICFB follow the instructions given below.

Go to "CIW" window and click *File -> Export -> Stream*. This opens the "Virtuoso Stream Out" window. Complete the form of "Virtuoso Stream Out" as shown in Fig1.

- Run Directory : .
- Library Name : cell (your library name)
- Top Cell Name : (leave blank)
- View Name: layout
- Output File: cell.gds (your .gds file)

r 😡	🥥 Virtuoso® Stream Out								
ок	Cancel	Defaults	Apply		Help				
User-Defi	ned Data	And Option	ns	User-Defined Data Options					
Template I	File	Load	Save	Ĭ					
				Library Browser					
Run Direct	tory				-				
Library Na	me			cell					
Top Cell Na	ame			¥.					
View Name	e			layoutž					
Output				🔶 Stream DB 🐟 ASCII Dump					
Output File	9			cell.gds]					
Scale UU/I	DBU			0.00100000 <u>i</u>					
Units				🔶 micron 					
Process N	ice Value	0-20		0					

Fig1: Virtuoso Stream Out

Creating LEF	
File	

In Fig 1 click *User-Defined Data*. The "Stream Out User-Defined Data" form opens as shown in Fig 2.

In Fig 2 enter stream.map for the Layer Map Table field. Then click OK.

Stream Out User-Defined Data								
OK Cancel Defaults Apply	Help							
Convert Pin to	🔶 geometry 🐟 text 🐟 drop							
Pin Text Map Table	<u>I</u>							
Keep pin information as attribute number	Q							
Cell Name Map Table	Ĭ.							
Layer Map Table	stream.map]							
Text Font Map Table	Ĭ.							
User-Defined Property Mapping File	).							
User-Defined Property Separator	,Ľ.							
User-Defined SKILL File	<u>.</u>							

Fig2: Stream Out User-Defined Data

The text file stream.map tells ICFB which layers correspond to which GDS numbers. When we re-import the GDS file back into Abstract Generator, the tech file we are going to use has the same layer mappings.

Now back in the "Virtuoso Stream Out" form (Fig 1), click *Options*. The "Stream Out Options" form opens as shown in Fig 3. In Fig3 select **Convert PCells to Geometry** field. This flattens out all parametric cells in the cell library (For the I/O Pad Cells). Change **Case Sensitivity** to **upper**. Then click *OK*.

Stream Out Options								
OK Cancel Defaults Apply	Help							
Report Bad Polygons								
To Use Parent XY for Text								
Output Rectangle as BOX								
Snap XY to Grid Resolution								
Convert Simple Mosaic to Array	<b>=</b>							
Convert PCells to Geometry	-							
Convert Lines to	🗢 path <> ignore							
Case Sensitivity	⇔preserve ♦upper ↓lower							
Convert Dots to	🔷 polygon 🐟 node 🔶 ignore							
Keep PCells								
Convert Paths to Polygons								
Library Version	5.0 =							
Precision Report								
Retain Reference Library (No Merge)								
	- X							

Fig3: Stream Out Options

Click *OK* in the "Virtuoso Stream Out" form. A "STRMOUT PopUp Message" appears showing some warnings as shown in Fig 4. You can ignore these warnings. In Fig 4 click *OK*. Thus a GDS file containing the standard cell library will be generated.

۲ <i>Q</i>	STRMOUT PopUp Message
2 mil)	<pre>PIPO STRMOUT (PID = ipc:2) completed successfully!! *** There were 0 error and 32 warning messages ***</pre>
	OK Cancel Help

Fig 4: STRMOUT PopUp Message

Tutorial 1 Release Date: 01/13/2005(Version 2) - 4 -

# **Initialize Abstract Generator:**

#### **Start the Abstract Generator:**

Go to your silicon ensemble directory and type the following command in the command prompt.

hostname.ece.pdx.edu >abstract -tech ./tech

The Abstract Generator window opens as shown in Fig 5.

		Abstra	.ct – [no c	urrent lib	rary]			
File Bins Ca	ells Flow							Help
			<i>¥</i>					
Bin	Cells	Cell	Layout	Logical	Pins	Extract	Abstract	Verify
Core	0							
10	0							
Corner	0							
Block	0							
Ignore	0							



#### Mapping the library to a particular technology file:

In the Abstract Generator you will have to add your library to the technology file (tech.dpux). This can be done by following the instructions given below.

In Fig 5 click *File -> Technology...* to bring up the "Technology File Editor" window. Under *Categories* (on the left), click *Library Path*. Click *Add* and replace *newLib1* with the name of your library (e.g. tut) and *newPath* with the path to your cadence library (e.g. /home/ece/siddhart/tut) as shown in Fig 6.

**Important Point**: MAKE ONE LIBRARY CONTAINING ALL STANDARD CELLS. The Silicon Ensemble abstract version of the cells will show up in ALL CAPS in Virtuoso, but the views will not be readable by Virtuoso. If your cells are named using ALL CAPS in Virtuoso, you will need to make a separate library directory for you abstract generator cells.

	Technology File Editor/tech/tech.dpux
File Edit Help	
Categories	Library Name File Path
Library Path Layers Inter Layers Vias Via Rules Routing Rules Grid Global	1     cell     /home/ece/siddhart/cell      Add       Delete

Fig 6: Technology File Editor – Library Path

In Fig 6 click *Layers*. Now Fig 6 appears as shown in Fig 7. In Fig 7 click *Mapping*. Now Fig 7 appears as shown in Fig 8.

Categories	Def	fine Ele	ctronic	Dis	splay Map	ping						
Library Path Layers		Layer	Туре		Class	Width	Sep.	Height	HeightSub	Extension		
nter Layers	1	nwell	MASK	T		3	0	0	0	-1	$\square$	Add
fias	2	nactive	MASK	•		1.2	0	0	0	-1		Delete
fia Rules	3	pactive	MASK	•		1.2	0	0	0	-1		
outing Rules and	4	poly	MASK	•	POLY 🚽	1.2	0	0	0	-1		
Global	5	cc	VIA	•	VIA0 🗸	0.6	0.9	0	0	-1		
	6	metal1	ROUTING	T	METAL1 💌	0.9	0.9	0	0	-1		
	7	via	VIA	•	VIA1 🗨	0.6	0.9	0	0	-1		
	8	metal2	ROUTING	•	METAL2 💌	0.9	0.9	0	0	-1		
	9	via2	VIA	•	VIA2 🗸	0.6	0.9	0	0	-1		
	10	metal3	ROUTING	•	METAL3 🗨	1.5	0.9	0	0	-1		
	11	pwell	GRAPHIC	▼	UNKNOWI	0	0	0	0	-1		

Fig 7: Technology File Editor - Layers

Tutorial 1 Release Date: 01/13/2005(Version 2)

In Fig 8 click *MAP*. A new window "Open" opens as shown in Fig 9. Then browse to get stream.map. Select stream.map and click *Open*. In the "Technology File Editor" window click *File -> Save* and close the "Technology File Editor" window by clicking *File -> Close*.

File Edit Help         Categories         Define       Electronic       Display       Mapping         Library Path         Layers       Inter Layer       Purpose       GDS         Inter Layers       1       25       0       cc       drawing       Map         Vias       Via Rules       48       0       cc       drawing       Add         Grid       5       9       0       metal1       drawing       Add         6       232       0       metal1       drawing       Delete         7       51       0       metal2       drawing       Delete         9       62       0       metal3       drawing       Delete         10       234       0       metal3       pin       Delete	<u>_</u>			Techno	logy File Editor-	/tech/tech.	dpux	
Categories       Define       Electronic       Display       Mapping         Library Path       Layers       Inter Layers       Image: Constraint of the second se	File Edit Help							
Library Path         Gds Number Gds Type         Layer         Purpose         GDS           Inter Layers         1         25         0         cc         drawing	Categories	Defi	ne Electro	onic Dis	splay Mapping			
Layers         Gds Number Gds Type         Layer         Purpose         GDS           Inter Layers         1         25         0         cc         drawing	Library Path			1				
Inter Layers       1       25       0       cc <ul> <li>drawing</li> <lidrawing< li=""> <li>dra</li></lidrawing<></ul>	Layers		Gds Number	Gds Type	Layer	Purpose	_ (	GDS
Vias       2       47       0       cc       drawing       Map         Via Rules       3       48       0       cc       drawing       Add         Grid       5       9       0       metal1       drawing       Add         6       232       0       metal1       pin       Delete         7       51       0       metal2       pin       g         9       62       0       metal3       pin       metal3         10       234       0       metal3       pin       metal3         11       42       0       nwell       drawing       Viawing	Inter Layers	1	25	0	CC 💌	drawing 🗨	<u>  </u>	
3       48       0       cc       drawing          Routing Rules       4       55       0       cc       drawing          Grid       5       49       0       metal1       drawing        Add         6       232       0       metal1       pin        Delete         7       51       0       metal2       pin           9       62       0       metal3       drawing           10       234       0       metal3       pin           11       42       0       nwell       drawing	Vias	2	47	0	cc 💌	drawing 🗨		Мар
4       55       0       cc       drawing       Add         Grid       5       49       0       metal1       drawing          6       232       0       metal1       pin        Delete         7       51       0       metal2       drawing         Delete         9       62       0       metal3       drawing             10       234       0       metal3       pin             11       42       0       nwell       drawing	Via Rules	3	48	0	cc 💌	drawing 🗨		
5       49       0       metal1       drawing	Routing Rules	4	55	0	cc 💌	drawing 🗨		Add
6       232       0       metal1       pin       Delete         7       51       0       metal2       drawing          8       233       0       metal2       pin          9       62       0       metal3       drawing          10       234       0       metal3       pin          11       42       0       nwell       drawing	Global	5	49	0	metal1 🗨	drawing 🗨		
7       51       0       metal2       drawing         8       233       0       metal2       pin         9       62       0       metal3       drawing         10       234       0       metal3       pin       metal3         11       42       0       nwell       drawing       metal3		6	232	0	metal1 🗨	pin 💌		Delete
8       233       0       metal2       pin		7	51	0	metal2 🗨	drawing 🗨		
9         62         0         metal3         drawing            10         234         0         metal3         pin            11         42         0         nwell         drawing		8	233	0	metal2 💌	pin 💌		
10         234         0         metal3         ■         pin         ■           11         42         0         nwell         ■         drawing         ✓		9	62	0	metal3 🗨	drawing 🗨		
11 42 0 nwell 🚽 drawing 🚽 🗸		10	234	0	metal3 🗨	pin 💌		
		11	42	0	nwell 👻	drawing 🚽		

Fig 8: Technology File Editor - Mapping

۲ <sup></sup>		Open	
<u>D</u> irectory:		/u/siddhart	- Ē
	r.run1 (a005525 (a005532 (a005542 (a005568 (a005696 (a005956	<ul> <li>XXa005964</li> <li>XXa005974</li> <li>XXa007658</li> <li>XXa007665</li> <li>XXa007674</li> <li>XXa0011935</li> <li>XXa019960</li> </ul>	È cellName.map È stream.map
File <u>n</u> a	ame: strea	ım.map	<u>Open</u>
Files of <u>t</u>	type: Gds	: Map File (*.map)	<u> </u>

Fig 9: Browsing for stream.map

Creating LEF	Tutorial 1
File	Release Date: 01/13/2005(Version 2)

# **Using Abstract Generator:**

Now we will be importing the GDS file exported earlier from Virtuoso. In the Abstract Generator window click *File -> Library*. Since you have only one library at this point it should come up automatically. If you have more than one library you should select the library you want to open. After the library opens the name of the Abstract Generator window changes to "Abstract-your library name". In our case the name of the Abstract Generator Generator window is "Abstract-tut".

In the "Abstract-tut" window click **File** -> *Import* -> *Stream(GDS11)*....The "Import Layout" window opens as shown in Fig 10. Browse until you find the GDS file you exported earlier from Virtuoso. Then click *OK*.

5	Import Layout	7
GDSII Filenames:		
/u/siddhart/tut.gds		Browse
Map GDSII names:	No Mapping 😑	
Default Bin:	Core 🛁	
1.	OK Cancel	Help

Fig 10: Import Layout

After a few moments the cells from your library will appear in the "Abstract-tut" window in Core Bin as shown in Fig 11.

「 <u>▼</u>	Abstract – tut								
File Bins C	File Bins Cells Flow Help								lelp
Bin	Cells	Cell	Layout	Logical	Pins	Extract	Abstract	Verify	
Core	6	AND	1						
10	0	AND_S_A_0	1						
Corner	0	INV	1						
Block	0	MUX	1						
Ignore	12	OR	1						
		OR_S_A_1	<ul> <li>✓</li> </ul>						

Fig 11: Abstract generator window after importing the gds file

At this point, if there are any cells that do not have a green tick next to them in the layout column, select them (Shift allows you to select groups, Control allows you to selector deselect one at a time...same as windows).When all the cells are selected click *Cells -> Move*. The "Move Select Cells" form opens as shown in Fig 12. Select **Ignore** and click *OK* to move these cells to the Ignore bin.

IC D	esign	and	Test
La	abora	tory	

Creating LEF	Tutorial 1
File	Release Date: 01/13/2005(Version 2)

Note: If there are cells without any valid views in the Core bin, you may not be able to export the library later.

	Move Selected C	ells <sup>–</sup>
To bin:	Core IO Comer Block Ignore	
OK	Cancel	Help

Fig 12: Move Selected Cells

There are three main steps in generating abstracts - generating the Pins view, the Extract view, and finally the Abstract view.

- The Pins step maps text labels to metal layers, designating certain metal blocks as pins (all pin information is lost during GDS export, so we need to re-instate that information).
- The Extract merges metal blocks under the same net into one single net
- The Abstract step copies the pin (net) information from the Extract step, and generated blockages for the metal and via layers (or any other layer that you specify). These blockages will tell the place-and-route tool (namely Silicon Ensemble) which parts of the standard cell to avoid routing over with certain layers.

The resulting Abstract view contains only net and blockage information, which will be exported into an LEF file and imported into Silicon Ensemble.

- 8 -

Creating LEF	Tutorial 1
File	Release Date: 01/13/2005(Version 2)

# Pins Step:

In Fig 11 select all the cells and click *Flow -> Pins*. The "Running step Pins for the selected cells(s)" form opens. Add all the output pins of all standard cells in the "Output pin names (regular expression)" as shown in Fig 13. Leave rest as default.

	Running step Pins for the selected cell(s)
Step	Map Text Boundary
🔶 Pins	Map text labels to pins:
	((text drawing) ( metal1 drawing) ( metal2 drawing ))
	Power pin names (regular expressions):
	vdd
	Ground pin names (regular expressions):
Bin	gnd
🔶 Core	
	Output pin names (regular expressions):
	0
	Run Cancel Help

Fig 13: Pins Step - Map

In Fig 13 click *Boundary* tab. Now the "Running step Pins for the selected cell(s)" window appears as shown in Fig 14.

- 9 -

Running step Pins for the selected cell(s)					
-Step	Map Text Boundary				
Pins	Create boundary:	as needed 💷			
	Using geometry on layers:				
	metal1 metal2 metal3 metal4 metal5 ia4 poly	via via2 via3 v			
	Adjust Boundary By				
	Left:				
	Right:				
BIN	Тор:				
Core	Bottom:				
	Fix Boundary To				
	Left:				
	Right:				
	Тор:				
	Bottom:				
	Run Ca	ncel Help			

Fig 14: Pins Step - Boundary

In Fig 14 click *Run*.

Now the "Abstract-tut" window appears as shown in Fig 15. For all the cells it should show a green tick in the Pins column. If it is shows ! sign there is some warning. If it shows a warning see the report.

To view the report click *Cells -> report*.

If there are no warnings the Pins step is over.

r 🔽	Abstract – tut							_
File Bins C	ile Bins Cells Flow Help							lelp
Bin	Cells	Cell	Layout Lo	ogical Pins	Extract	Abstract	Verify	
Core	6	AND						
IO	0	AND_S_A_0						
Corner	0	INV						
Block	0	MUX						
Ignore	12	OR						
		OR_S_A_1		× .				

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Creating LEF	Tutorial 1
File	Release Date: 01/13/2005(Version 2)

#### **Extract Step:**

In Fig 15 select all the cells in the "Abstract-tut" window and click *Flow ->Extract*. The "Running step Extract for the selected cell(s)" window opens as shown in Fig 16.

~~r	Signal Power Antenna
Pins	Extract signal nets
Extract	Extract through layers:
	metal1 metal2 metal3 metal4 metal5 via via2 via
	104
	Extract through weak layers:
	Restrict pins to layers:
	metal1 metal2 metal3 metal4 metal5 via via2 via
	184
	,
	Extract Limitations
Core	Maximum depth: 20
	Maximum distance:
	Minimum width:
	Create Must Connect Pins If Required
	_ Always
	Only on terminals named:

Fig 16: Extract step - Signal

In Fig 16 click on the Power tab and select Extract Power Nets as shown in Fig 17.

- 11 -



Tutorial 1 Release Date: 01/13/2005(Version 2)

Running step Extract for the selected cell(s)					
Step	Signal Power Antenna				
<ul> <li>Pins</li> <li>Extract</li> </ul>	<ul> <li>Extract power nets</li> <li>Extract through layers: metal1 metal2 metal3 metal4 metal5 via via2 via3 v ia4 Restrict pins to layers: metal1 metal2 metal3 metal4 metal5 via via2 via3 v ia4         </li> </ul>				
Bin Core	Extract Limitations         Maximum depth:       20         Maximum distance:				
	Run Cancel Help				

Fig17: Extract step - Power

Then click *Run*. The "Abstract-tut" window should appear as shown in Fig 18. All the cells should have a green tick in the Extract column. If there are ! signs in the Extract column then there are some warnings. To see the warnings view the report by clicking *Cell -> report*. If there are no warnings then the Extract step is over.

	S Abstract – tut							
File Bins C	ells Flow						Help	)
Bin	Cells	Cell	Layout Logical	Pins	Extract	Abstract	Verify 🔼	ſ
Core	6	AND						
10	0	AND_S_A_0	$\checkmark$	1	$\checkmark$			
Corner	0	INV	$\checkmark$	1	1			
Block	0	MUX	$\checkmark$	1	$\checkmark$			
Ignore	12	OR	$\checkmark$	1	$\checkmark$			
		OR_S_A_1	✓	1	<ul> <li>Image: A second s</li></ul>		17	í

Tutorial 1 Release Date: 01/13/2005(Version 2)

Fig 18: Abstract generator after Extract Step

#### **Abstract Step:**

Now select each cell one by one and follow the procedure given below. After selecting the standard cell click *Flow -> Abstract* in Fig 18. The "Running step Abstract for the selected cell(s)" window opens as shown in Fig 19.

	Adjust	Blockage	Site	Overlap	Grids	
ins	—Signal N	lote				
xtract	- Signal I	to houndary :	nine			
ural i		te nonunar à l	huis			
	Power N	lets				
	🔲 Crea	te boundary	pins			
	🔟 Crea	te ring pins				
	Ring pin	max distanc	e to bound	lary:		
	Power g	jeometry gro	ups:			single
	Only cre Don't cr	eate pins whi reate pins wh	ch overlap ich overla	o geometry p geometry	on layer p y on layer	urposes purposes
	Only cre Don't cr	eate pins whi eate pins wh	ch overlap ich overla	o geometry p geometry	on layer p y on layer	urposes: purposes
	Only cre Don't cr	eate pins whi eate pins wh ee Geometry	ch overlap ich overla	o geometry	on layer p y on layer	urposes: purposes
	Only cro Don't cr 45 Degr Stair-s' Stair-s'	eate pins whi reate pins wh ee Geometry tep coverage teps width:	ch overlap ich overla :	o geometry	on layer p y on layer ( 0.45	urposes: purposes partial



Creating LEF	Tutorial 1	- 14 -
File	Release Date: 01/13/2005(Version 2)	

In Fig 19 click on *Site* tab, enter *core* for the Site Name as shown in Fig 20. Site core is used for cells inside the pad frame that are 18um high and multiple of 2.4um wide.

Site dbl\_core is for cells 36um high and multiple of 2.4um wide. Sites IO and corner describe components of the pad frame.

	Running step Abstra	act for the selected	cell(s)
Step	Adjust Blockage	Site Overlap	Grids
Pins	Site Name:		core
✓ Extract ♦ Abstract			
Bin			
🔶 Core			
		(	
		Run	Cancel Help
L			<u>ل</u> ے

Fig 20: Abstract step - Site

In Fig 20 click on **Grids** tab fill the form as shown in Fig 21 (NOTE: All units in um).

Tutorial 1 Release Date: 01/13/2005(Version 2)

Step	Adjust Blockage Site Overlap	Grids
Pins     Eutmot	Grid analysis mode:	report 🔤
Abstract	Save routing grids to technology file	
	Routing Grid Values	
	Metal1 pitch:	1.5
	Metal1 offset:	0.75
	Metal2 pitch:	1.5
	Metal2 offset:	0.75
	Routing Grid Calculation Maximum metal1 pitch (% above line to v Maximum metal2 pitch (% above line to v	ria): 50
	Pin access mode:	normal 💻
Bin	🔲 Adjust boundary width	
🔶 Core	Adjust boundary height	
	_ Require diagonally adjacent vias	quelideon

Fig 21: Abstract step - Grids

In Fig 21 click *Run* to generate the abstract view of standard cell. Repeat this procedure for all the standard cells. After the Abstract step is over for all the cells the "Abstract-tut" window appears as shown in Fig 22. For all the cells the Abstract column should will have a ! sign.

Creating LEF	Tutorial 1 -
File	Release Date: 01/13/2005(Version 2)

	v Abstract – tut								-
File Bins C	ells Flow							He	ilb 🛛
		• 🛛 🔤 🛯	9						
Bin	Cells	Cell	Layout	Logical	Pins	Extract	Abstract	Verify	A
Core	6	AND							
IO	0	AND_S_A_0							
Corner	0	INV							
Block	0	MUX							
Ignore	12	OR							
		OR_S_A_1	4		- <b>-</b>	$\checkmark$			7

Fig 23: Abstract Generator after Abstract step

To view report click *Cell -> report* in "Abstract-tut" window. The Report should be as shown in Fig 24.

r"	Report – AND
Info:	created pin "A" for label "A" at (-6450,-6600)
Info:	created pin "A" for label "A" at (-6450,8550)
Info:	created pin "B" for label "B" at (-4050,8550)
Info:	created pin "B" for label "B" at (-4050,-6600)
Info:	created pin "0" for label "0" at (3150, -6600)
Info:	created pin "0" for label "0" at (3150,8550)
Info:	created pin "gnd!" for label "gnd!" at (-8550,-4500)
Info:	created pin "vdd!" for label "vdd!" at (-8400,6600)
Info:	8 pins created
Extract	status: 0k
Info:	extracting 5 nets
Info:	using preset pins on net A, 1 of 5
Info:	extracting net gnd!, 2 of 5
Info:	using preset pins on net B, 3 of 5
Info:	extracting net vdd!, 4 of 5
Info:	using preset pins on net 0, 5 of 5
Abstract	status: Warn
Info:	Rail gnd!, calculated width = 1.2 microns, offset = -4.95 microns
Info	Rail vdd!, calculated width = 1.2 microns, offset = 5.85 microns
Warning:	Terminal vdd! has no pins on Metall-Metal2 Routing grid
Warning:	Terminal gnd! has no pins on Metall-Metal2 Routing grid
Warning:	requires different site definition from that associated with Core bin
Verify	status: None
	X
	OK < > Help
i	

Fig 24: Final Report

NOTE: The warning under the Abstract step should state that vdd! and gnd! have no pins on the Matal1-Metal2 routing grid .These should be ignored. If there are warnings for the other pins, they should be taken care of by placing the pins on the intersection of metal1 and metal2 routing grids in the standard cell layout as shown below (Fig 25).

16 -

Tutorial 1 Release Date: 01/13/2005(Version 2)

			Virtuos	so® La	iyout Ea	liting: te	st in	v layout			
<b>X:</b> 1	7.875	Y: 14.	175	(F) \$	Select: O	d)	X: 1.8	375	dY: 1.4	425	6
Tools	Desigr	Window	Create	Edit	Verify	Connecti	vity	Options	Route	NCSU	
		0.7	500	. 71				<b>E00</b> 07E0			$\cdot \Delta$
à		· 1.5	۵۰۰۰ <del>۱</del>	0, 73 		000 88.50 242 88 88 88					
e e		1.5	. 1 2006.								
			- 0								
<u> </u>		1.5	:00Q _								•
				<u>X////////////////////////////////////</u>							
		1.5	- 0000 1								
Q		<sup>-</sup> 1.5	000 -								
<i>"</i>		1.5	006 _								
			· •		·						•
문문		1.5	000g _		ø						
1111F		1.5	് രാവം								
<u>8</u> 62				Q. 75	500 <u>al. 5</u>	000 31 50	000 1	. 5000750			
<u> </u>		0.7	500 –			2.2 2.2 2.2 2.2 2 2.2 2 2 2 2 2 2 2 2 2					
S.			-0			88					7
[abcd]	Mouse I	: Enter B	Point	1	M: Pop-1	up Menu		R: Tog	gle L90	) X/Y	
	Point at	the first p	oint of th	ne ruler	n i						

Fig 25: Layout showing routing grid rules

# **Cell Orientation:**

In the "Abstract-tut" window select all the standard cells and click *Cells -> Cell Properties*. A "Cell Properties" window opens as shown in Fig 26. Change **class** to **symmetry** and **R0** to **X** and click *Apply*. Then click *OK*.

Creating LEF	Tutorial 1
File	Release Date: 01/13/2005(Version 2)

Change property	symmetry 🛁 to	×	Apply
Cell			
	Bin	class	symmetry
AND	Core	CORE	X
AND_S_A_0	Core	CORE	
INV	Core	CORE	
мих	Core	CORE	Х
OR	Core	CORE	Х
OR_S_A_1	Core	CORE	Х

Fig 26: Cell Properties

### LEF File:

There is one last step before exporting the LEF file. In the "Abstract-tut" window select *File -> General Options*. The "General Options" window opens as shown in Fig 27. In Fig 27 select **Silicon Ensemble** for **Target place and route system**, **1000** for **LEF units**, and **5.3** for **LEF version**. Click *OK*.

Gener	al Options
General Views	
Target place and route system:	Silicon Ensemble 💷
Default Bin:	Core 💻
LEF Units:	1000 =
LEF Version:	5.3 💻
01	Cancel Help

Fig 27: General Options

In the "Abstract-tut" window click *File -> Export -> LEF* to bring up the "Export LEF" form as shown in Fig 28.

Specify the location of where you wish to save the file.

Select **Core** for the **Export LEF for Bin** field and click *OK*. Close the "Abstract-tut" window.

Σ	Export LEF		
LEF Filename:			
abstract, lef			Browse
LEF Units:		1000 —	4
LEF Version:		5.3 –	4
Export LEF for Bin:		Ali –	4
🔟 Export Antenna LEF			
Antenna LEF Filename:			
antenna.lef			
		(	
	ок	Cancel	Help

Fig 28: Export LEF

This is the end of creating the LEF File.

# LEF CORRECTION

Go to your silicon ensemble directory and run the perl script lef\_correction on your LEF file. Type this command .

*hostname.ece.pdx.edu* > *lef\_corrections* your\_*file\_name.lef* > *new\_file\_name.lef*.

### **Reason for LEF file correction:**

The abstract views created in the Abstract Generator renamed the cells to ALL CAPS. Because Cadence is case sensitive, you will need to go back and replace these capitalized names (in the LEF file exported from Abstract Generator) with the original, lower-case cell names used in Virtuoso.

Thus the LEF file has been created. Now you can proceed with any one of the following approaches.

- 1) Create a verilog netlist from the schematic (Tutorial 2).
- 2) Create DEF file from the schematic (Tutorial 3).