Introduction:

These tutorials are developed by the Department of Electrical and Computer Engineering of Portland State University on 13th January 2004. They are intended for students studying IC Design using NCSU CDK Design kit 1.3. The Cadence tools used are IC 5.0 and LDV 4.1. These tutorials are intended for standard cell and custom (involving standard cells and transistors) designs using Automatic Placement and Routing tool (Silicon Ensemble). The main purpose of these tools is time saving. We have successfully done automatic placement and routing of a design involving 200 gates (9K transistors) in 21 sec. Refer to the setup for the requirements of the files needed for the automatic placement and route tools. In these tutorials we have tried to consolidate the effort of various prior tutorials into a single tutorial.

Automatic Placement and Route Flow:

Placement and Routing using verilog netlists can be used for designs involving standard cells and custom designs (Tutorial 1, 2, 4). Placement and Routing using DEF file (Tutorial 1, 3, 5) can be used for designs involving only standard cells.

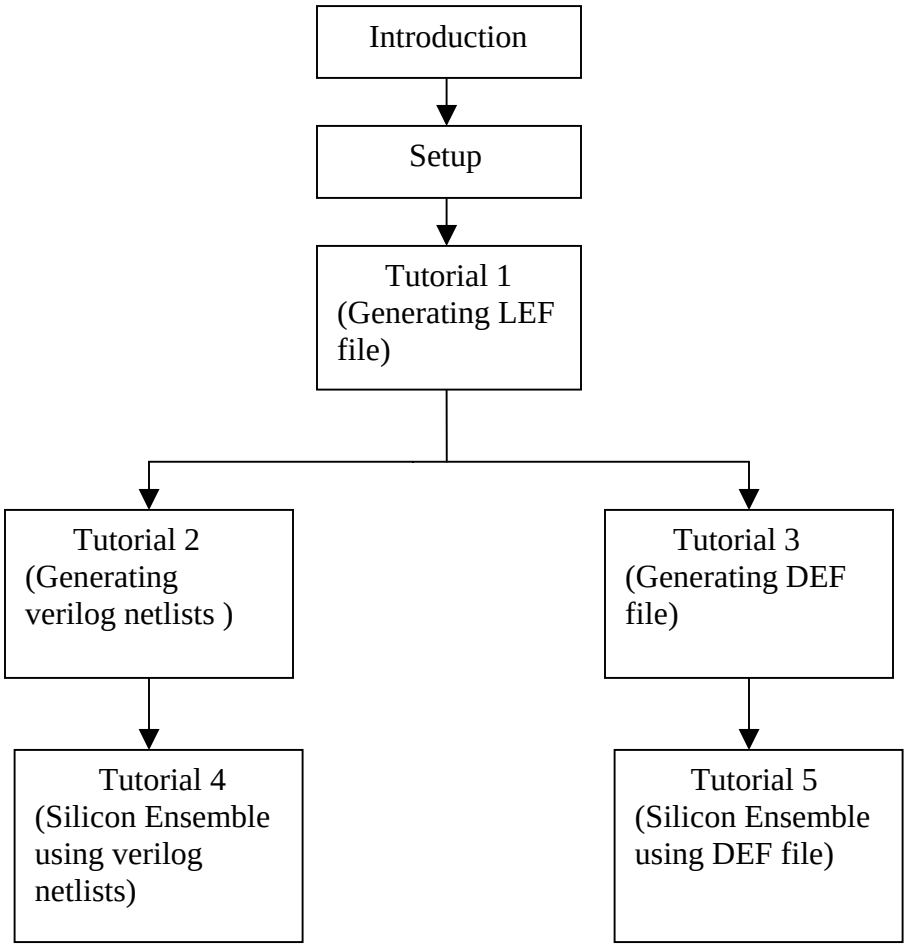

Fig 1: Tutorial Flow

Mixed (Standard Cell and Transistors) Based Automatic Placement and Routing using Silicon Ensemble:

Make separate standard cells and verilog netlists for nmos and pmos (Tutorial 2) and follow the same procedure as given in the standard cell based automatic placement and routing tutorial (Tutorial 4).

NOTE: Tutorials 3 and 5 do not work for IC 5.0.

Conventions used in the tutorials:

Buttons in the form - Italics Bold
Field names - Bold
Form names - Quotes
Typing in the form or command prompt – Italics

Glossary:

NCSU: North Carolina State University.
CDK: Cadence Design Kit.
ICFB: Integrated Circuit Front to Back.
LEF: Library Exchange Format.
DEF: Design Exchange Format.
DRC: Design Rule Check.
LVS: Layout versus Schematic.