Syllabus ECE426/526 Winter 2007
8 January 2007

Instructor: W. Robert Daasch, daasch@ee.pdx.edu, FAB 160-14, 503.725.5409
Office Hours: Tu,Th 2:00PM to 4:00PM and by appointment
Text: *CMOS VLSI Design, 3nd Edition*, Weste and Harris
Others: *CMOS Digital Integrated Circuits (Analysis and Design), 2nd Ed*,
Kang and Leblebici
Digital Integrated Circuits, A Design Perspective, J.M. Rabaey
VLSI Design Techniques for Analog and Digital Circuits, Gieger, Allen and Strader.
The Modern VLSI Design, W. Wolf
The Design and Analysis of VLSI Circuits, L. Glasser and D. Dobberpuhl

Course URL: http://ece.pdx.edu/~daasch/course/x26
Streaming URL: http://www.media.pdx.edu
Textbook URL: http://www.cmosvlsi.com/

Deadline for forming and approval of laboratory team is January 15th, MLK holiday.

This is the second term of an approved two term undergraduate sequence and an approved three term graduate sequence. The second term's goals are to apply the results of last term's study of MOSFET gates and use them in small design problems; to introduce the steps used in floor-planning of digital subsystems and circuits; and introduce the study of test and manufacturability of digital MOS circuits. A laboratory is integrated into the lecture. Students will gain skills in device and small scale integrated circuit simulation and, CMOS IC layout.

Basic Coverage:

Chapter 7, Sequential Circuit Design; This chapter is review as well completing coverage of the material not covered in Fall 2005.

Chapter 8, Design Methodology and Tools; Each design style has its advantages Delay, Power, Time to market etc.

Chapter 9, Testing and Verification; To a point the ideal performance of simulation is all that is needed to realize a functional circuit. To realize a manufacturable circuit requires considerably more testing than is included in the text.

Chapter 10 Data-path Subsystems; A host of logic functions such as addition, multiplication, comparators etc. provide the foundation for regular and structured VLSI design.

Chapter 11 Array Subsystems: A common ASIC in 2004 has more area dedicated to memory (SRAM) than logic. Local memory improves performance, increases flexibility and increases the test complexity.

Chapter 12, Special-purpose Subsystems: Circuitry for Inputs and Outputs (I/Os), power distribution, clock distribution and packaging to hold it all completes the design of a VLSI system.

Design Tools:	Cadence IC Design Tools Integrated Circuit Front to Back (icfb);
Technology:	The course objectives will focus on system design and integration and less on specific gates. N-well TSMC CMOS design rules are used in the laboratory.
Background:	1 high level programming language, logic design, MOS electronics. Prerequisites ECE 425
Laboratory:	Anyone new to the course this term that does not have a department account (do not use a ECE 20x, ECE 30x account for this class) should secure from the CAT an assigned account before next week.

There are 4 laboratories this term. submitted one per team of (2 or 3 students). Overcrowding in the VLSI Laboratory this term is likely. Laboratory seat time may have to be assigned (if so, times to be arranged). The Fourth Avenue labs are open to EE/CpE students from 8am - 6pm Monday through Friday. Students in 426/526 should refrain from using the Tektronics Circuits lab. ECE x26 students should recognize that the labs are not a private laboratory, a self-imposed maximum of 2-3 hrs per sitting.

Grading:

Students will be graded by 400 pts.; midterm is 100 pts, the 4 labs normalized at the end of the quarter to combined 100 pts. and a final is 200 pts. Exams are closed book and no notes. No Make-up exams are and excused exams must be arranged in advance.

Separate grade scales will be set for ECE 426 and ECE 526.

A total score of 95% or more is assigned a grade of *A*. For an average number of points, the grade will range between B^- to B^+ depending on class performance. A total score of less than 50% will be assigned a grade no higher than C^-. As determined by the instructor a failing percentage may be set and graded with an *F*.