Scan Latch
Laboratory 2
ECE 426/526
11 February 2007

Laboratory 2 builds upon Laboratory 1 with the design of common cell that supports scan testing of digital integrated circuits. The cell uses the laboratory D-latch (master) adding combinational logic multiplexor to this D-input, and a second D-latch (slave).

Each standard cell has a data-sheet with a cell description, logic equations, truth table, performance characteristics, schematic and polygon layout. This data-sheet is the basis of laboratory reports.

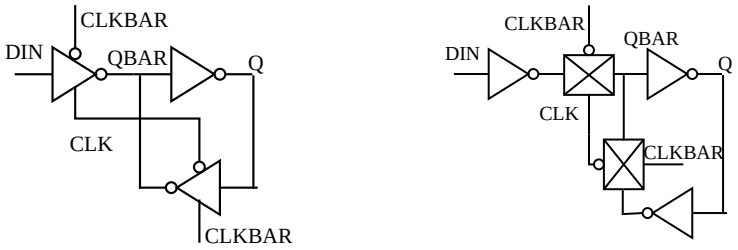
A report template of the data-sheet is completed and submitted for each cell. The "Standard Cell Report Template" is located at

http://ece.pdx.edu/~daasch/course/x25/lab/Full_Datasheet.doc

The goals for this laboratory are

- Build upon understanding of CMOS circuits and systems
- Select a CMOS design of a scan master-slave
- Create a schematic and physical layout of selection
- Verify function of schematic and physical layout
- Modify prototype to meet specifications
- Document final design

It is recommended that you use a the base the same latch that your team selected for Laboratory 1.



A drive inverter (output buffer) for *Q* is recommended.

Design logic and physical design of CMOS Scan Master-Slave for an external output load capacitor equal to FO4.

- Label the inputs “DIN”, “TI” test input, “TE” test enable, “CLK” and “CLKBAR” and the output “Q”.
- Include both types of ohmic contacts to the physical design.
- All transistors should be minimum length.
- Test enable is active high *TE=1* for storing the data from signal *TI*. Test enable low *TE=0* for storing the data from signal *DIN*.

Complete the following components of the data-sheet template for scan master-slave standard cell.

Cell Description, Cell Symbol, Cell Truth Table, Cell Schematic Diagram, Cell Lay-out

Performance Analysis; Q (only) rise and fall, propagation tables for DIN to Q (only) and TI to Q (only), and propagation equations for these data to output paths.

Add a table summarizing the latch setup and latch hold times.