D-Latch
Laboratory 1
ECE 426/526
28 January 2007

Laboratory 1 continues from Fall 2006 with the design of an additional small standard cell. For Winter 2007 the standard cell design is a D-latch with asynchronous reset.

Standard cells are common in integrated circuit design. A standard cell typically uses transistors larger than the minimum size to permit the cell's output to be connected the inputs of five or 10 other standard cells. The layout arrangement of cell input and output are fixed to ease the use of CAD such as placement and route.

Each standard cell has a data-sheet with a cell description, logic equations, truth table, performance characteristics, schematic and polygon layout. This data-sheet is the basis of laboratory reports.

A report template of the data-sheet is completed and submitted for each cell. The "Standard Cell Report Template" is located at

http://ece.pdx.edu/~daasch/course/x25/lab/Full_Datasheet.doc

The goals for this laboratory are

Build upon understanding of CMOS circuits and systems

Select a CMOS design prototype for a D-latch

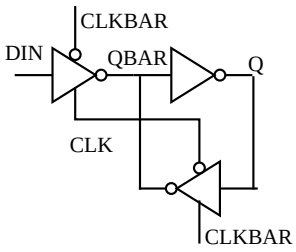
Create a schematic and physical layout of selection

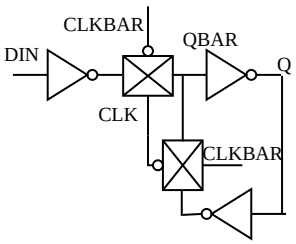
Verify function of schematic and physical layout

Modify prototype to meet specifications

Document final design

Select one of the D-latch examples for your base D-latch schematic.





A drive inverter (output buffer) for *Q* is recommended.

Design logic and physical design of CMOS D-latch for an external output load capacitor equal to FO4 (using your group inverter) propagation times approximately 3X your inverter.

Label the inputs "DIN", "RESET", "CLK" and "CLKBAR" and the output "Q" and "QBAR".

Include both types of ohmic contacts to the physical design.

All transistors should be minimum length.

Reset is active high *RESET=1* for output *Q=0*.

Complete the following components of the data-sheet template for D-latch standard cell.

Cell Description, Cell Symbol, Cell Truth Table, Cell Schematic Diagram, Cell Lay-out

Performance Analysis; Q (only) rise and fall, propagation tables for DIN to Q (only) and CK to Q (only), Propagation Delay Equations

Add a table summarizing the latch setup and latch hold times.