Digital Integrated Circuit Design II ECE 426/526 Announcements

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12 March 2007

- □ Final Exam 19 March 2007, 3:30 to 5:30 PM
 - In class URBN 204
 - Format similar to all other exams
 - Chapters 8, 9, 10, 11, 12 (12.1 12.4 excluding optional sections)

5 March 2007

- □ Lab two grades will go out tonight
- Laboratory 3 should be in and establish that all teams are generating netlists and driving place and route
- □ No class 7 March 2007
- There will be one make up tape on IO circuits available after 9 March

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- There will be one make up tape on IO circuits available after 9 March
- □ Personal observation for Laboratories 3 & 4
 - When it comes to Verilog-XL and Silicon Ensemble

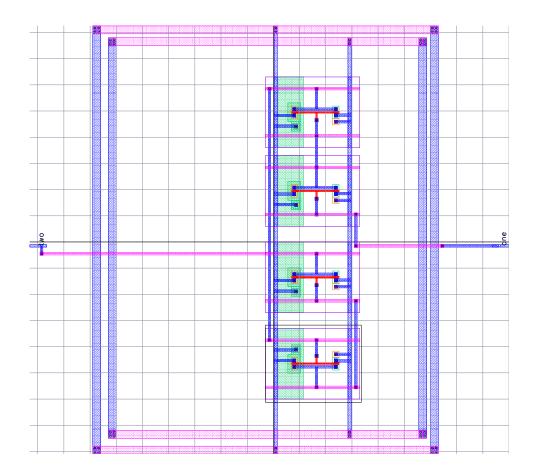
many libraries $H^3 \Leftrightarrow$ Headache, Heartburn and Hassle

- □ Midterm grading done and returned today
 - Midterm averages: ECE 425 = 77, ECE 525 = 83
- □ Laboratory 3 and 4 are combined
 - Comparison of ripple and carry-lookahead out soon
 - Two designs each with scan chain
 - Scan chain links inputs and outputs of the adder A, B, and S

$$S = A + B$$

- S is 9 bits, A and B are 8 bits each
- Simulation is Verilog-XL with timing added for each standard cell

□ Place and route is up and running. Yippeeee!



Example Layout

- Getting the place and route to run meant not enough time to finish the grading
- The netlist generation and P&R tutorials are largely correct.
 - Some of the screen shots are from older versions of the tool
 - The new view is abstract which can be run off the Solaris command line
 - The only flow change is you don't have to import standard cell GDS into abstract
 - Assuming layout views for each standard cell the layout view can be used for PIN abstraction

- □ Midterm returned on Wednesday
- Laboratory 3 requires place and route and is up.
 Hopefully bugs are removed

- □ Laboratory 1 grades distributed today
- Place and Route is perfect yet. Hold on for day or two of Laboratory 3.
- □ Midterm Examination 14 February 2007
 - Location: normal classroom URBN 204
 - o full class period 4:00PM to 5:50PM
 - Crib sheet on cover of exam only. Closed notes and text
 - o Chapters 8,9, 10.1, 10.2

- □ Midterm Examination 14 February 2007
 - Chapters 8, 9, and 10 to coverage this week
 - Attendence will set the level of mid-term and final partial credit
- □ Laboratory 2: Scan chains
 - Do not typically have a rese
 - Replace a reset with the scan in
 - Assume static logic forms (no domino multi-clock etc.)

- Second lab requires the use of the placement and routing there are some problems with the new version that we are work hard to correct
- □ Ankita Satta has been assigned for TA
 - Email: ankita@ece.pdx.edu
 Lab Hours: W 2-4PM and Friday 3-5PM
- □ Email subject lines
 - General "Subject: ECE x26"
 - Laboratory sumission "Subject: ECE x26 Group x Laboratory y
- □ Forward or read your user@ece.pdx.edu address
- □ Google listserv is available

http://groups.google.com/group/pdx_ecex26/

To (hopefully) encourage signups I will check at least once a week and post information

- □ No TA has been assigned
- If no TA is assigned (it they probably won't be) laboratories can only be minimally supported during lecture and office hours
- Arrange to read email sent to your ECE account. This is the only email account that course related information will be sent to.
- If you read email using a different account forward the ECE email.
- Be sure to submit the names of your laboratory team (sized at three) by 15 January 2007 No smaller groups will be allowed without prior written approval
- If you are not on a team on January 15th you will be assigned at random.

- First Laboratory is available Thursday http://ece.pdx.edu/~daasch/course/x26
 - Final Standard Cell is a D-latch
- Complete the Tutorials for Place and Route you will need them for laboratories 2, 3 and 4
- Request for office appointment for a time less than 24 hours away is rarely granted.
- Shown dates and times are for scheduled appointments.
 Appointment details are screened from the web