

MS Thesis defense by John Alfredo
“A Trace Cache for Embedded Real-Time Systems”
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Advisor: Dr. Douglas Hall

Abstract

Many low-end embedded systems run sophisticated applications via an RTOS, despite the fact that these systems have relatively unsophisticated hardware features. These systems typically lack branch prediction logic, and as a result suffer branch delay penalties. At most these systems have small caches of 4K to 16K bytes.

One of the main benefits often stated for the trace cache in the Intel Pentium processor is the caching of decoded CISC instructions. This project will demonstrate that a trace cache is beneficial even in a pure RISC environment.

A trace cache in an ARM7-style simulator is shown to significantly reduce the branch delay penalty without the use of either a branch predictor or a second level instruction cache. A hit rate of 98.39% is achieved on a 4K byte trace cache for a speedup of 1.085 over that of a conventional instruction cache of the same size. Novel search techniques are used to enhance the hit rate of the trace cache.